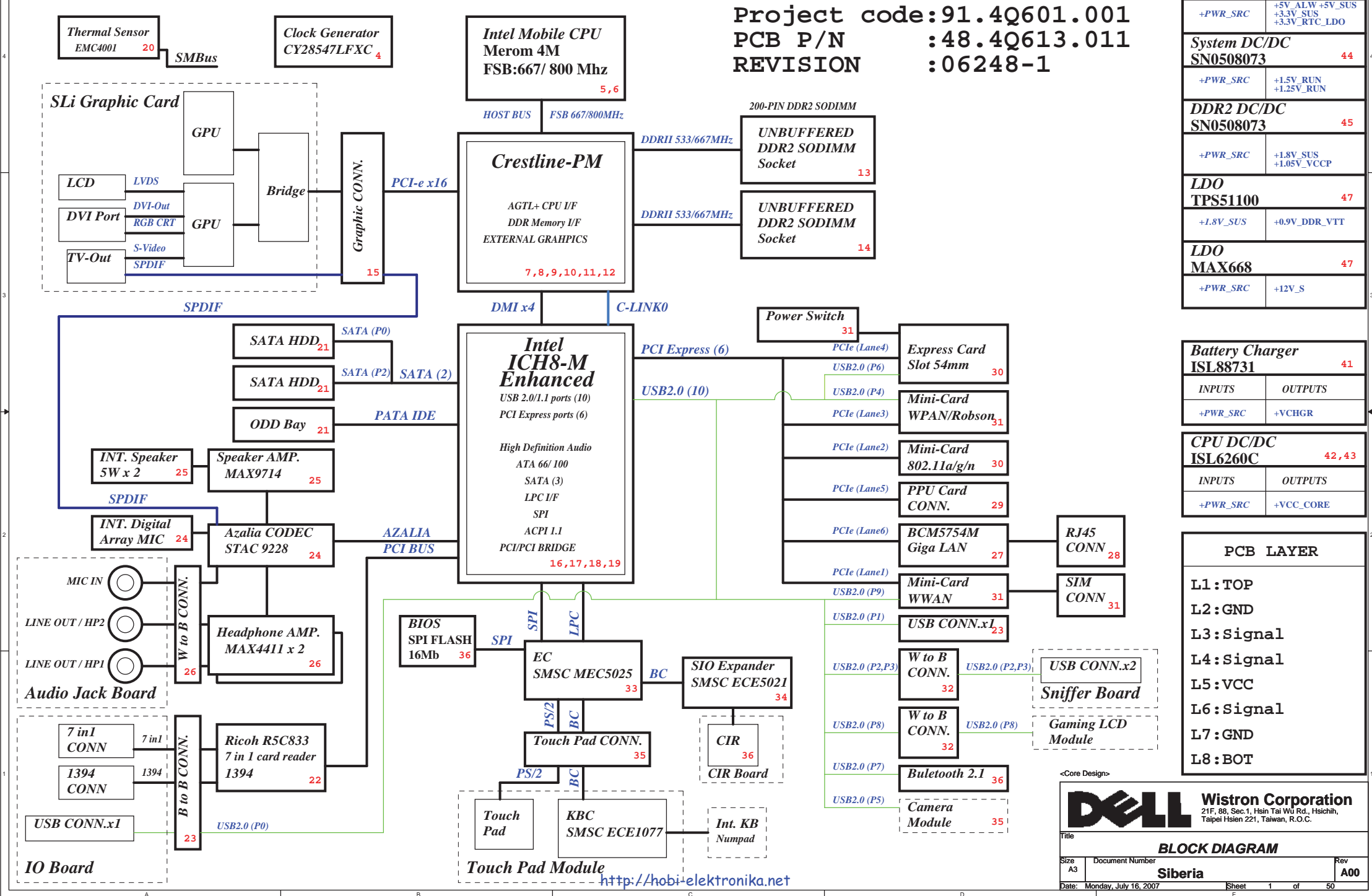


Siberia Block Diagram



CLOCK GEN CY28547

27M_SS/LCD96_100M SELECTION TABLE

BYTE 10

Bit5 S1	Bit4 S0	Spread Spectrum S[1:0]
0	0	-0.5%(Default)
0	1	-1.0%
1	0	-1.5%
1	1	-2.0%

BYTE 15
IO_VOUT[2,1,0]

Bit2 IO_VOUT2	Bit1 IO_VOUT1	Bit0 IO_VOUT0	IO_VOUT[2,1,0]
0	0	1	0.3V
0	0	0	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V(Default)
1	1	0	0.9V
1	1	1	1.0V

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order) ★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reserved	Normal Operation ★	Lane Reserved
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation ★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA	NO SDVO Card Present ★	SDVO Card Present

CFG 12	XOR/ALL-Z
CFG 13	Reserved
LL(00)	Reserved
LL(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

PCIE Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	BT/UWB/Robson
LANE4	Express Card
LANE5	PPU card
LANE6	Giba Bit LOM

PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD17	C D	1	1

USB TABLE

ICH

USB0	Ext Lift Side
USB1	Ext Back
USB2	Ext Right Side (Top)
USB3	Ext Right Side (Bottom)
USB4	3rd mini card
USB5	Camera
USB6	Express Card
USB7	BT
USB8	Gaming LCD
USB9	WWAN

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved. Rising Edge of PWROK.	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap		
ICH_RSVP_P3	AZ_DOUT ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable	high = default
BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

Integrated VccSus1_05,VccSus1_5,VccCL1_5		
SM_INTVRMEN	High=Enable	Low=Disable
Integrated VccLAN1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaulte
	High=No Reboot

8.2K PULL HIGH

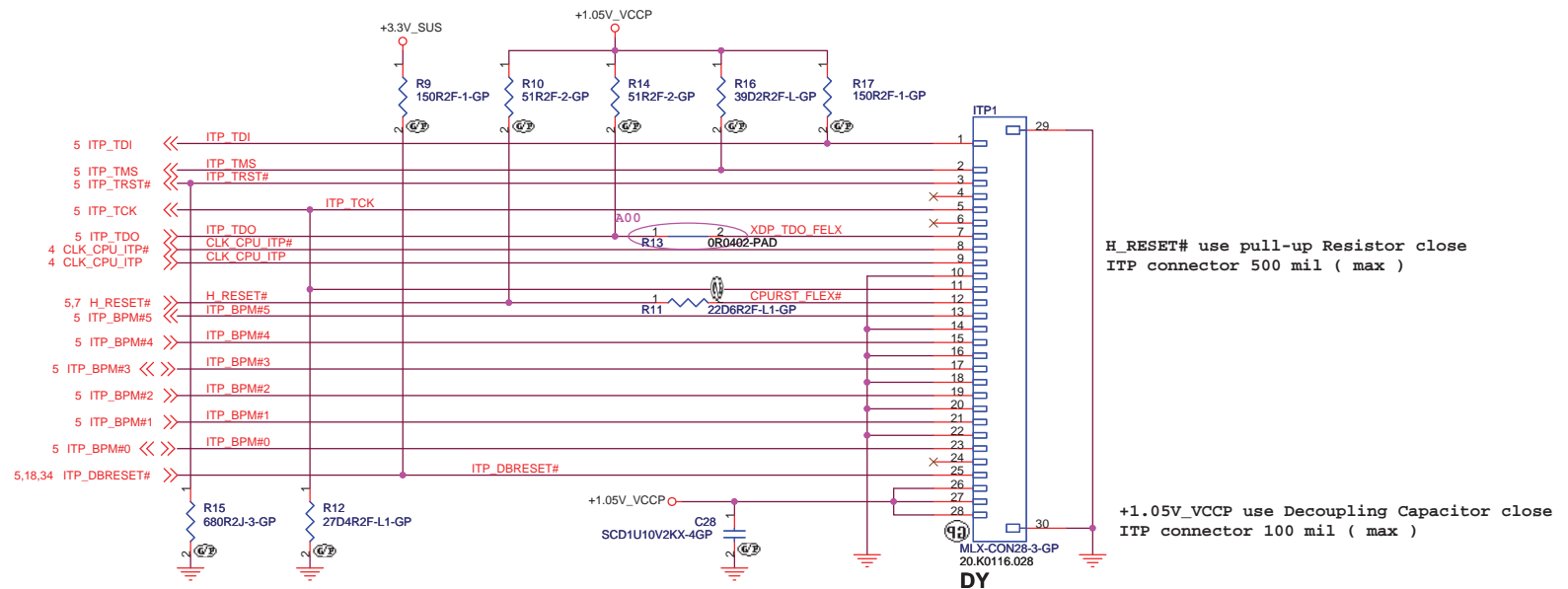
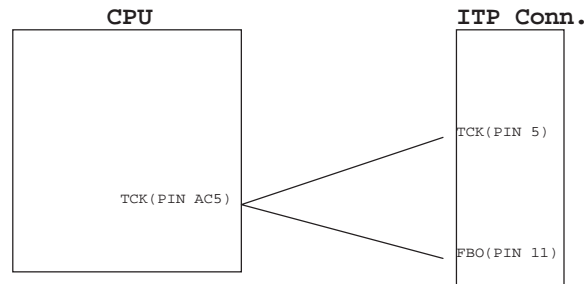
INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST0#	PULL-UP 13K

Core Design

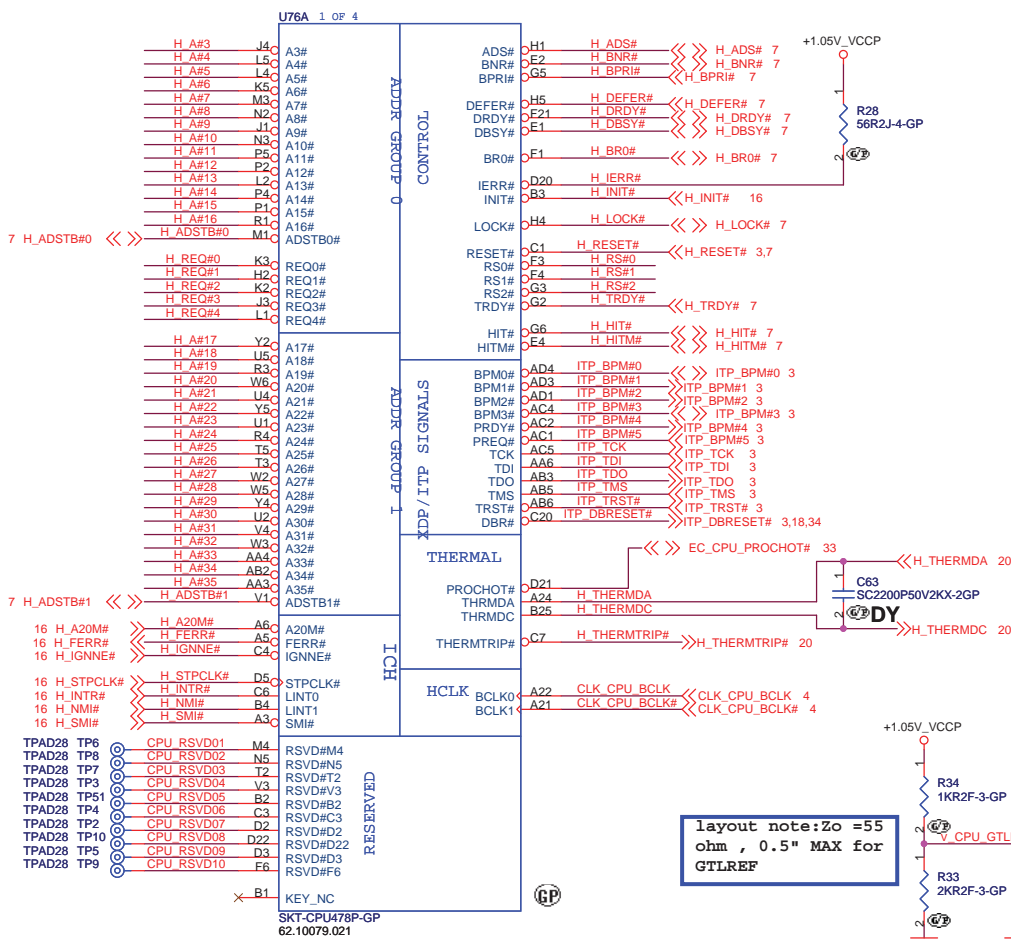
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Table of Content		
Size A3	Document Number Siberia	Rev A00
Date: Monday, July 16, 2007	Sheet 2 of 50	

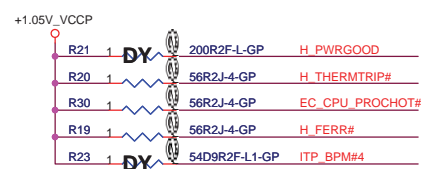


ITP Debug Conn.

H_D#[63..0] << >> H_D#[63..0] 7
H_A#[35..3] << >> H_A#[35..3] 7
H_REQ#[4..0] << >> H_REQ#[4..0] 7
H_RS#[2..0] << >> H_RS#[2..0] 7



Use old Symbol replace New P/N
original value:MEROM-CPU479P-GP-U



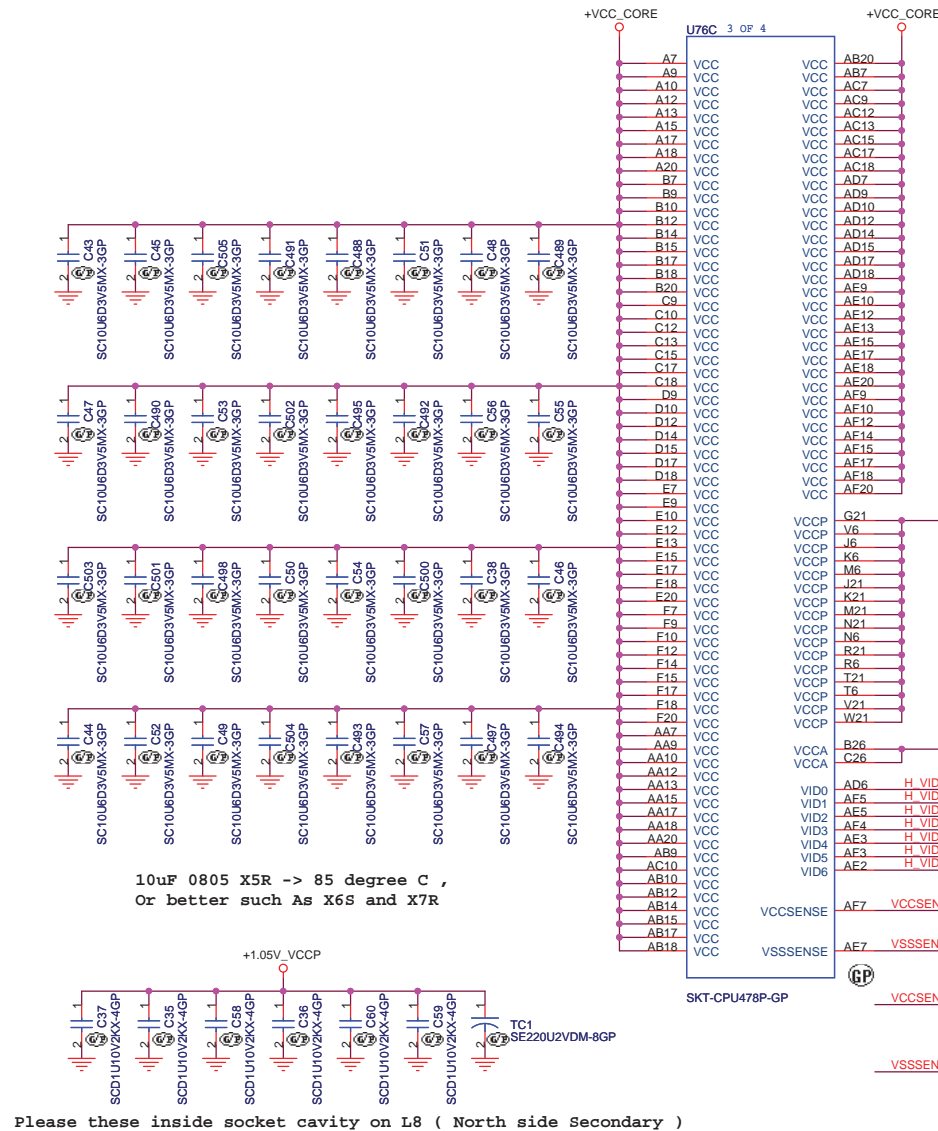
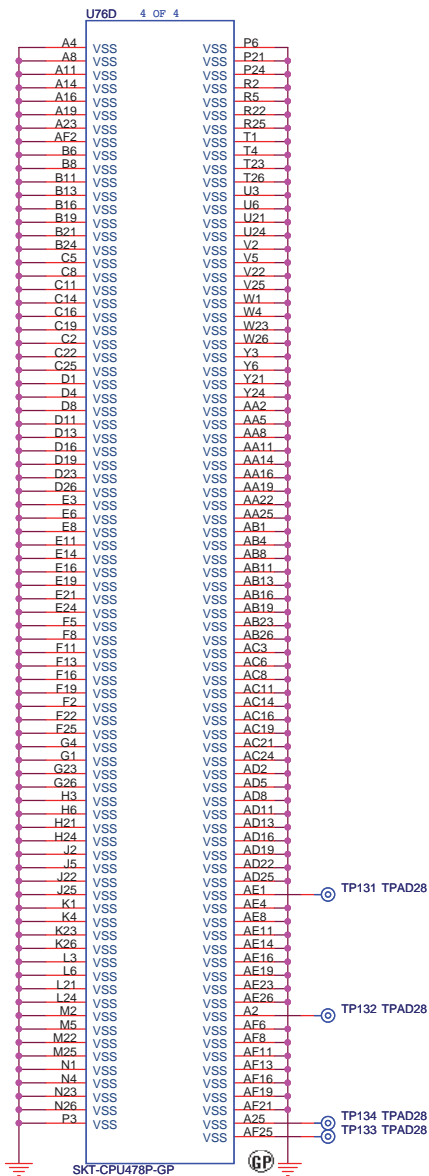
PLACE C66 close to the TEST4 PIN,
make sure TEST4 PIN routing is
reference to GND and away from
other noisy signals

TPAD28 TP11 TEST3
TPAD28 TP1 TEST5
For the purpose of testability,
route the signals through a ground
referenced Zo=55ohm trace that ends
in a via that is near a GND via
and is accessible through an
oscilloscope connection.



Note:
H_DPRSTP# need to daisy chain
from ICH8 to IMPV6 to CPU

Make COMP[3..0] traces length shorter
than 0.5". Trace should be at least 25
mils away from any other toggling
signal.
COMP 0,2 connect Zo=27.4ohm.
COMP 1,3 connect Zo=55ohm.



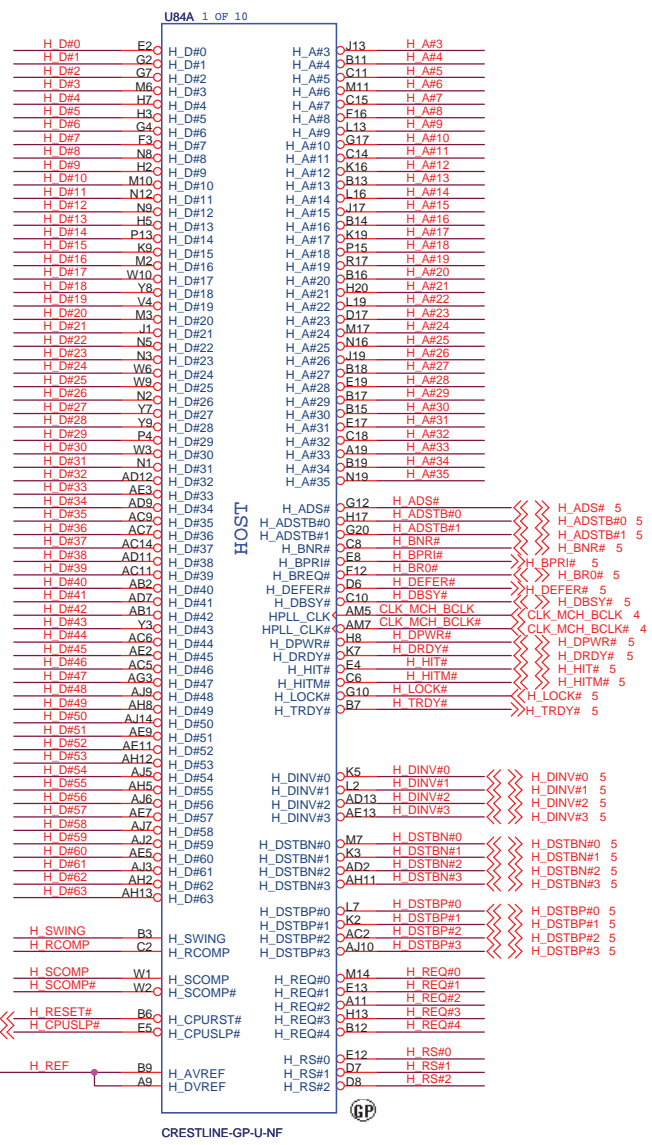
<Core Design>



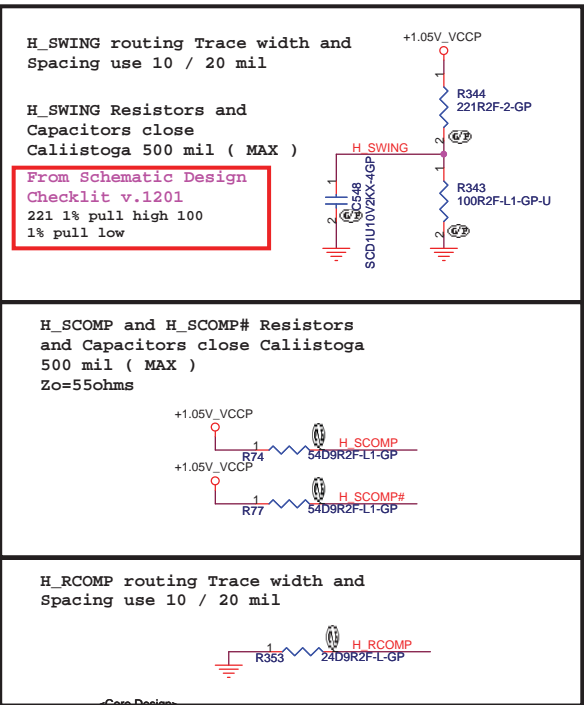
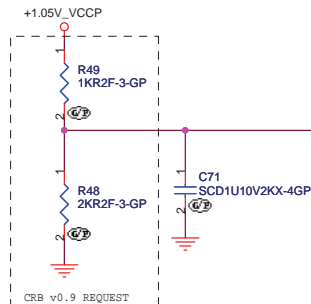
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

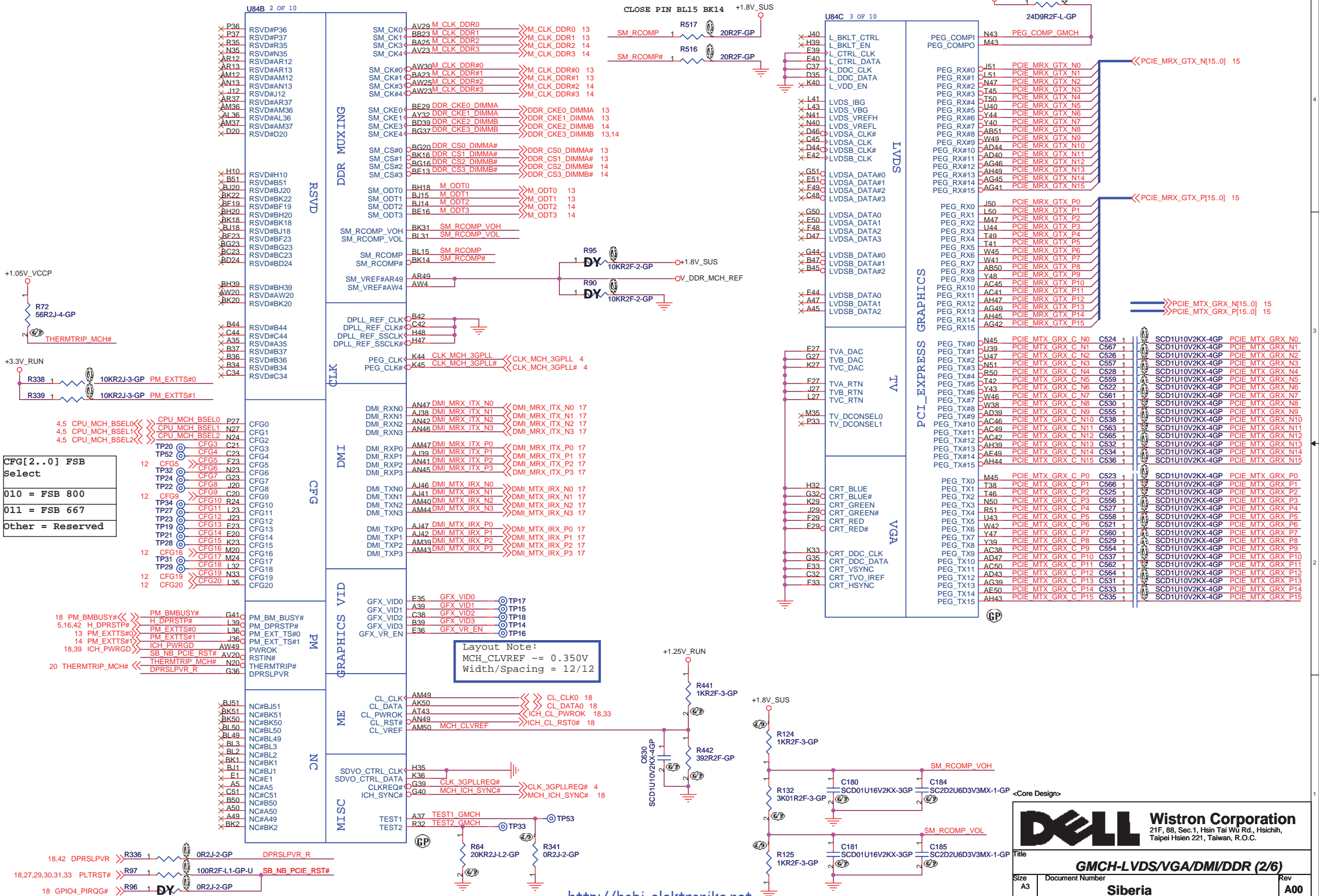
Title				
CPU-POWER (2/2)				
Size	Document Number			Rev
A3	Siberia			A00
Date:	Monday, July 16, 2007		Sheet	6 of 50

H_D#[63..0] << >> H_D#[63..0] 5
H_A#[35..3] << >> H_A#[35..3] 5
H_REQ#[4..0] << >> H_REQ#[4..0] 5
H_RS#[2..0] >>> H_RS#[2..0] 5



H_REF Decoupling Crestline
close Crestline 100 mil





CFG[2..0] FSB Select	
010	= FSB 800
011	= FSB 667
Other	= Reserved

Layout Note:
MCH_CLVREF ~ 0.350V
Width/Spacing = 12/12



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
GMCH-LVDS/VGA/DMI/DDR (2/6)		
Size A3	Document Number	Rev A00
Siberia		
Date: Monday, July 16, 2007	Sheet 8	of 50

DDR A D[63..0] << >> DDR_A_D[63..0] 13
DDR A BS[2..0] >>> DDR_A_BS[2..0] 13,14
DDR A DM[7..0] >>> DDR_A_DM[7..0] 13
DDR A DQS[7..0] << >> DDR_A_DQS[7..0] 13
DDR A DQS#[7..0] << >> DDR_A_DQS#[7..0] 13
DDR A MA[14..0] >>> DDR_A_MA[14..0] 13,14

U84D 4 OF 10

DDR A D0	AR43	SA_DQ0	SA_BS0	BB19	DDR A BS0
DDR A D1	AW44	SA_DQ1	SA_BS1	BK19	DDR A BS1
DDR A D2	BA45	SA_DQ2	SA_BS2	BF29	DDR A BS2
DDR A D3	AY46	SA_DQ3			
DDR A D4	AR41	SA_DQ4	SA_CAS#	BL17	DDR A CAS#
DDR A D5	AR45	SA_DQ5			
DDR A D6	AT42	SA_DQ6			
DDR A D7	AW47	SA_DQ7	SA_DM0	AT45	DDR A DM0
DDR A D8	BB45	SA_DQ8	SA_DM1	BD44	DDR A DM1
DDR A D9	BF48	SA_DQ9	SA_DM2	BD42	DDR A DM2
DDR A D10	BG47	SA_DQ10	SA_DM3	AW38	DDR A DM3
DDR A D11	BJ45	SA_DQ11	SA_DM4	AW13	DDR A DM4
DDR A D12	BB47	SA_DQ12	SA_DM5	BG8	DDR A DM5
DDR A D13	BG50	SA_DQ13	SA_DM6	AY5	DDR A DM6
DDR A D14	BH49	SA_DQ14	SA_DM7	AN6	DDR A DM7
DDR A D15	BE45	SA_DQ15			
DDR A D16	AW43	SA_DQ16	SA_DQS0	AT46	DDR A DQS0
DDR A D17	BE44	SA_DQ17	SA_DQS1	BE48	DDR A DQS1
DDR A D18	BG42	SA_DQ18	SA_DQS2	BB43	DDR A DQS2
DDR A D19	BE40	SA_DQ19	SA_DQS3	BC37	DDR A DQS3
DDR A D20	BE44	SA_DQ20	SA_DQS4	BB16	DDR A DQS4
DDR A D21	BH45	SA_DQ21	SA_DQS5	BH6	DDR A DQS5
DDR A D22	BG40	SA_DQ22	SA_DQS6	BB2	DDR A DQS6
DDR A D23	BF40	SA_DQ23	SA_DQS7	AP3	DDR A DQS7
DDR A D24	AR40	SA_DQ24	SA_DQS#0	AT47	DDR A DQS#0
DDR A D25	AW40	SA_DQ25	SA_DQS#1	BD47	DDR A DQS#1
DDR A D26	AT38	SA_DQ26	SA_DQS#2	BC41	DDR A DQS#2
DDR A D27	AW36	SA_DQ27	SA_DQS#3	BA37	DDR A DQS#3
DDR A D28	AW41	SA_DQ28	SA_DQS#4	BA16	DDR A DQS#4
DDR A D29	AY41	SA_DQ29	SA_DQS#5	BH7	DDR A DQS#5
DDR A D30	AV38	SA_DQ30	SA_DQS#6	BC1	DDR A DQS#6
DDR A D31	AT38	SA_DQ31	SA_DQS#7	AP2	DDR A DQS#7
DDR A D32	AV13	SA_DQ32			
DDR A D33	AT13	SA_DQ33	SA_MA0	BJ19	DDR A MA0
DDR A D34	AW11	SA_DQ34	SA_MA1	BD20	DDR A MA1
DDR A D35	AV11	SA_DQ35	SA_MA2	BK27	DDR A MA2
DDR A D36	AU15	SA_DQ36	SA_MA3	BH28	DDR A MA3
DDR A D37	AT11	SA_DQ37	SA_MA4	BL24	DDR A MA4
DDR A D38	BA13	SA_DQ38	SA_MA5	BK28	DDR A MA5
DDR A D39	BA11	SA_DQ39	SA_MA6	BJ27	DDR A MA6
DDR A D40	BE10	SA_DQ40	SA_MA7	BJ25	DDR A MA7
DDR A D41	BD10	SA_DQ41	SA_MA8	BL28	DDR A MA8
DDR A D42	BD8	SA_DQ42	SA_MA9	BA28	DDR A MA9
DDR A D43	AY9	SA_DQ43	SA_MA10	BC19	DDR A MA10
DDR A D44	BG10	SA_DQ44	SA_MA11	BE28	DDR A MA11
DDR A D45	AW5	SA_DQ45	SA_MA12	BG30	DDR A MA12
DDR A D46	BD7	SA_DQ46	SA_MA13	BJ16	DDR A MA13
DDR A D47	BB9	SA_DQ47	SA_MA14	BJ29	DDR A MA14
DDR A D48	BB5	SA_DQ48			
DDR A D49	AY7	SA_DQ49	SA_RAS#	BE18	DDR A RAS#
DDR A D50	AT5	SA_DQ50	SA_RCVEN#	AY20	M A RCVEN#
DDR A D51	AT7	SA_DQ51			
DDR A D52	AY6	SA_DQ52	SA_WE#	BA19	DDR A WE#
DDR A D53	BB7	SA_DQ53			
DDR A D54	AR5	SA_DQ54			
DDR A D55	AR8	SA_DQ55			
DDR A D56	AR9	SA_DQ56			
DDR A D57	AN3	SA_DQ57			
DDR A D58	AM6	SA_DQ58			
DDR A D59	AN10	SA_DQ59			
DDR A D60	AT9	SA_DQ60			
DDR A D61	AN9	SA_DQ61			
DDR A D62	AM9	SA_DQ62			
DDR A D63	AN11	SA_DQ63			

CRESTLINE-GP-U-NF



DDR B D[63..0] << >> DDR_B_D[63..0] 14
DDR B BS[2..0] >>> DDR_B_BS[2..0] 14
DDR B DM[7..0] >>> DDR_B_DM[7..0] 14
DDR B DQS[7..0] << >> DDR_B_DQS[7..0] 14
DDR B DQS#[7..0] << >> DDR_B_DQS#[7..0] 14
DDR B MA[14..0] >>> DDR_B_MA[14..0] 13,14

U84E 5 OF 10

DDR B D0	AP49	SB_DQ0	SB_BS0	AY17	DDR B BS0
DDR B D1	AR51	SB_DQ1	SB_BS1	BG18	DDR B BS1
DDR B D2	AW50	SB_DQ2	SB_BS2	BG36	DDR B BS2
DDR B D3	AW51	SB_DQ3			
DDR B D4	AN51	SB_DQ4	SB_CAS#	BE17	DDR B CAS#
DDR B D5	AN50	SB_DQ5			
DDR B D6	AV50	SB_DQ6	SB_DM0	AR50	DDR B DM0
DDR B D7	AV49	SB_DQ7	SB_DM1	BD49	DDR B DM1
DDR B D8	BA50	SB_DQ8	SB_DM2	BK45	DDR B DM2
DDR B D9	BB50	SB_DQ9	SB_DM3	BL39	DDR B DM3
DDR B D10	BA49	SB_DQ10	SB_DM4	BH12	DDR B DM4
DDR B D11	BE50	SB_DQ11	SB_DM5	BJ7	DDR B DM5
DDR B D12	BA51	SB_DQ12	SB_DM6	BF3	DDR B DM6
DDR B D13	AY49	SB_DQ13	SB_DM7	AW2	DDR B DM7
DDR B D14	BF50	SB_DQ14			
DDR B D15	BF49	SB_DQ15	SB_DQS0	AT50	DDR B DQS0
DDR B D16	BJ50	SB_DQ16	SB_DQS1	BD50	DDR B DQS1
DDR B D17	BJ44	SB_DQ17	SB_DQS2	BK46	DDR B DQS2
DDR B D18	BJ43	SB_DQ18	SB_DQS3	BK39	DDR B DQS3
DDR B D19	BL43	SB_DQ19	SB_DQS4	BJ12	DDR B DQS4
DDR B D20	BK47	SB_DQ20	SB_DQS5	BL7	DDR B DQS5
DDR B D21	BK49	SB_DQ21	SB_DQS6	BE2	DDR B DQS6
DDR B D22	BK43	SB_DQ22	SB_DQS7	AV2	DDR B DQS7
DDR B D23	BK42	SB_DQ23	SB_DQS#0	AU50	DDR B DQS#0
DDR B D24	BJ41	SB_DQ24	SB_DQS#1	BC50	DDR B DQS#1
DDR B D25	BL41	SB_DQ25	SB_DQS#2	BL45	DDR B DQS#2
DDR B D26	BJ37	SB_DQ26	SB_DQS#3	BK38	DDR B DQS#3
DDR B D27	BJ36	SB_DQ27	SB_DQS#4	BK12	DDR B DQS#4
DDR B D28	BK41	SB_DQ28	SB_DQS#5	BK7	DDR B DQS#5
DDR B D29	BJ40	SB_DQ29	SB_DQS#6	BF2	DDR B DQS#6
DDR B D30	BL35	SB_DQ30	SB_DQS#7	AV3	DDR B DQS#7
DDR B D31	BK37	SB_DQ31			
DDR B D32	BK13	SB_DQ32	SB_MA0	BC18	DDR B MA0
DDR B D33	BE11	SB_DQ33	SB_MA1	BG28	DDR B MA1
DDR B D34	BK11	SB_DQ34	SB_MA2	BG25	DDR B MA2
DDR B D35	BC11	SB_DQ35	SB_MA3	AW17	DDR B MA3
DDR B D36	BC13	SB_DQ36	SB_MA4	BF25	DDR B MA4
DDR B D37	BE12	SB_DQ37	SB_MA5	BE25	DDR B MA5
DDR B D38	BC12	SB_DQ38	SB_MA6	BA29	DDR B MA6
DDR B D39	BG12	SB_DQ39	SB_MA7	BC28	DDR B MA7
DDR B D40	BJ10	SB_DQ40	SB_MA8	AY28	DDR B MA8
DDR B D41	BL9	SB_DQ41	SB_MA9	BD37	DDR B MA9
DDR B D42	BK5	SB_DQ42	SB_MA10	BG17	DDR B MA10
DDR B D43	BL5	SB_DQ43	SB_MA11	BE37	DDR B MA11
DDR B D44	BK9	SB_DQ44	SB_MA12	BA39	DDR B MA12
DDR B D45	BK10	SB_DQ45	SB_MA13	BG13	DDR B MA13
DDR B D46	BJ8	SB_DQ46	SB_MA14	BE24	DDR B MA14
DDR B D47	BJ6	SB_DQ47			
DDR B D48	BF4	SB_DQ48	SB_RAS#	AV16	DDR B RAS#
DDR B D49	BH5	SB_DQ49	SB_RCVEN#	AY18	M B RCVEN#
DDR B D50	BG1	SB_DQ50			
DDR B D51	BC2	SB_DQ51	SB_WE#	BC17	DDR B WE#
DDR B D52	BK3	SB_DQ52			
DDR B D53	BE4	SB_DQ53			
DDR B D54	BD3	SB_DQ54			
DDR B D55	BJ2	SB_DQ55			
DDR B D56	BA3	SB_DQ56			
DDR B D57	BB3	SB_DQ57			
DDR B D58	AR1	SB_DQ58			
DDR B D59	AT3	SB_DQ59			
DDR B D60	AY2	SB_DQ60			
DDR B D61	AY3	SB_DQ61			
DDR B D62	AU2	SB_DQ62			
DDR B D63	AT2	SB_DQ63			

CRESTLINE-GP-U-NF

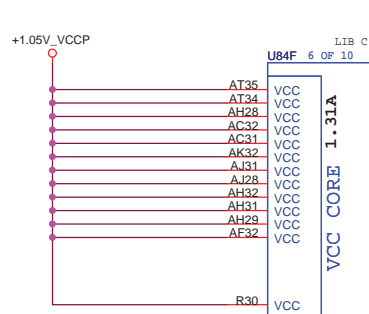


<Core Design>

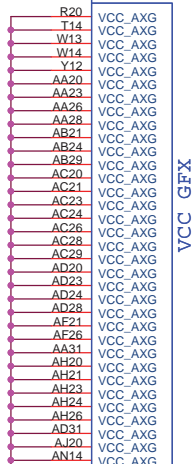
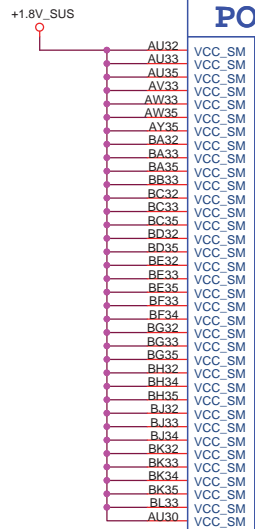


Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

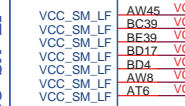
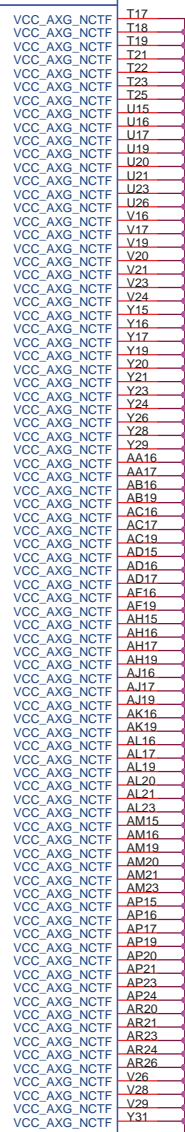
Title		
GMCH-DDR (3/6)		
Size	Document Number	Rev
A3	Siberia	A00
Date: Monday, July 16, 2007		Sheet 9 of 50



POWER

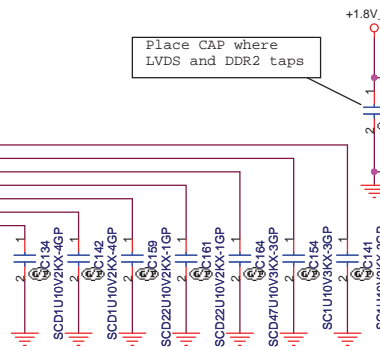


CRESTLINE-GP-U-NF



Supply	Signal Group	Icc-max
+1.05V_VCCP	VCC	1.31A
+1.05V_VCCP	VCC_NCTF	A
+1.05V_VCCP	VTT	0.85A
+1.05V_VCCP	VCC_PEG	1.2A
+1.05V_VCCP	VCC_RXR_DMI	0.25A
+1.05V_VCCP	VCC_ATX	84.15mA
+1.8V_SUS	VCC_SM	2.4A
+1.8V_SUS	VCC_SM_CK	0.2A
+1.25V_RUN	VCCA_HPLL	0.05A
+1.25V_RUN	VCCA_MPLL	0.15A
+1.25V_RUN	VCCA_SM	0.735A
+1.25V_RUN	VCCA_SM_NCTF	A
+1.25V_RUN	VCCA_SM_CK	0.015A
+1.25V_RUN	VCCD_HPLL	0.25A
+1.25V_RUN	VCCA_AXD	0.2A
+1.25V_RUN	VCCA_AXD_NCTF	A
+1.25V_RUN	VCCA_PEG_PLL	0.1A
+1.25V_RUN	VCCA_PEG_PLL	0.35A
+1.25V_RUN	VCCA_AXF	0.1A
+1.25V_RUN	VCCA_DMI	0.1A
+1.5V_RUN	VCCD_TVDAC	0.06A
+3.3V_RUN	VCCA_PEG_BG	0.005A
+3.3V_RUN	VCC_HV	0.1A

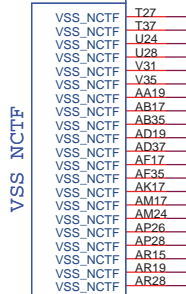
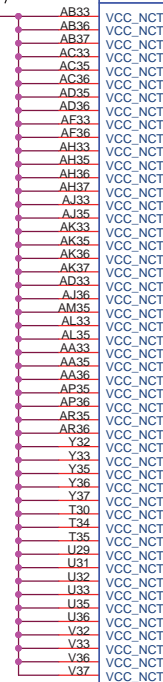
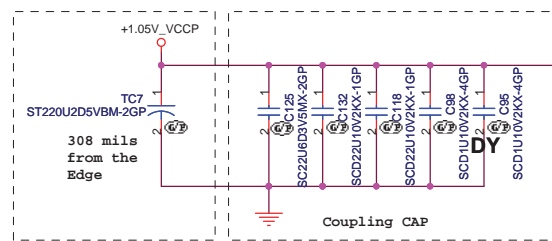
Place CAP where LVDS and DDR2 taps



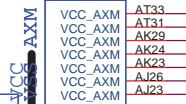
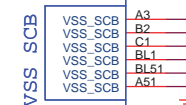
<http://hobi-elektronika.net>



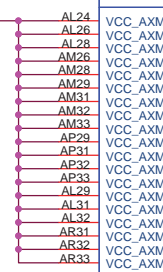
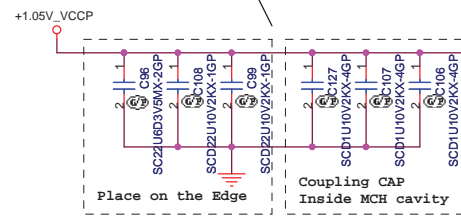
FOR VCC CORE AND VCC NCTF



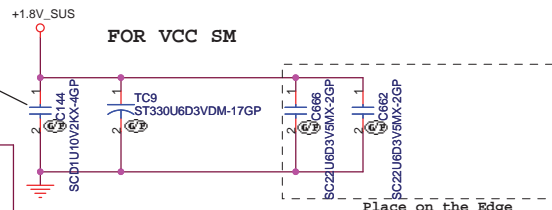
POWER



FOR VCC AXM NCTF AND VCC AXM



FOR VCC SM



<Core Design>



Title			GMCH-POWER (4/6)		
Size	Document Number			Rev	A00
A3	Siberia				
Date:	Monday, July 16, 2007	Sheet	10	of	50

8 CFG19 >> CFG19 1 R337 100nF 4K02R2F-GP +3.3V_RUN

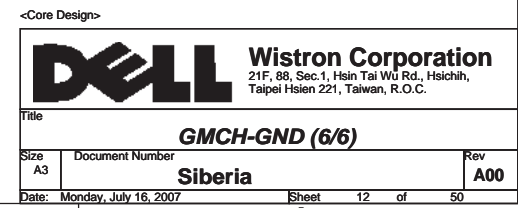
8 CFG20 >> CFG20 1 R340 100nF 4K02R2F-GP

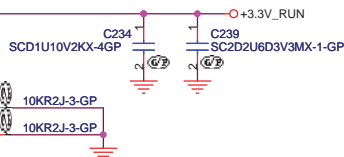
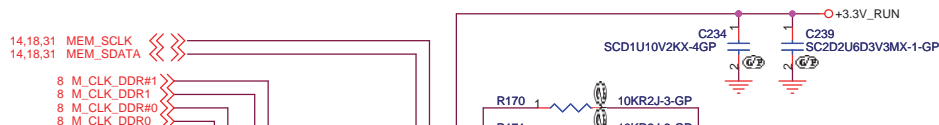
8 CFG5 >> CFG5 1 R58 100nF 4K02R2F-GP

8 CFG9 >> CFG9 1 R342 100nF 4K02R2F-GP

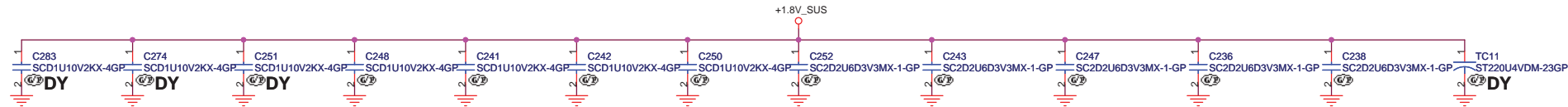
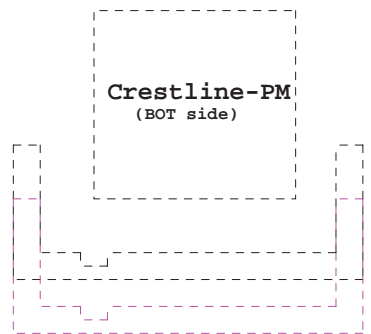
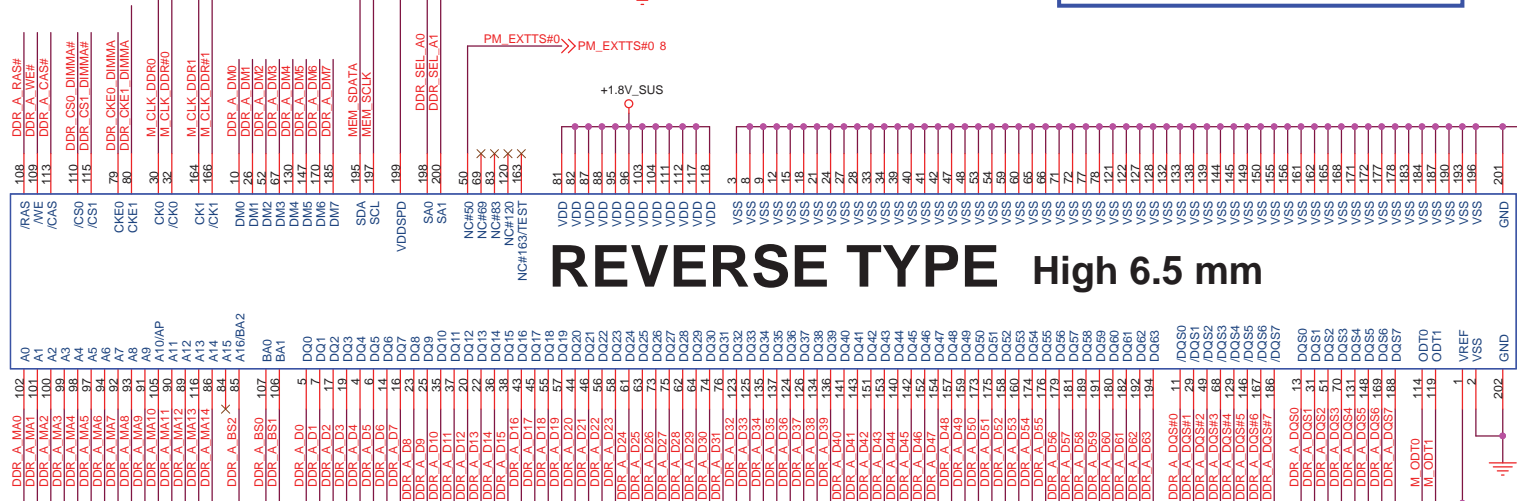
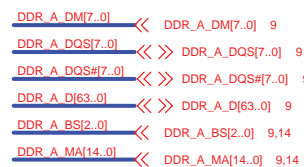
8 CFG16 >> CFG16 1 R63 100nF 4K02R2F-GP

<http://hobi-elektronika.net>

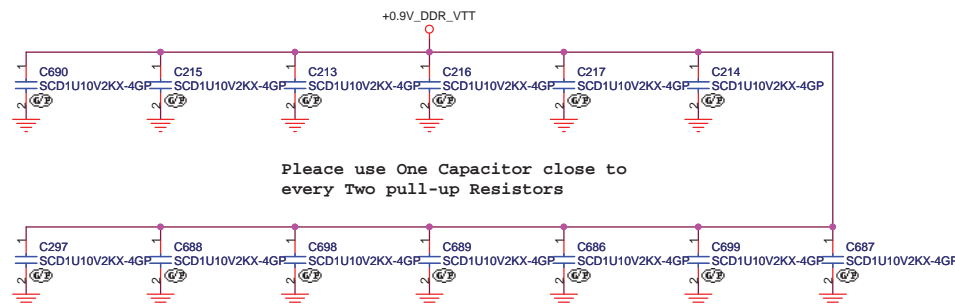




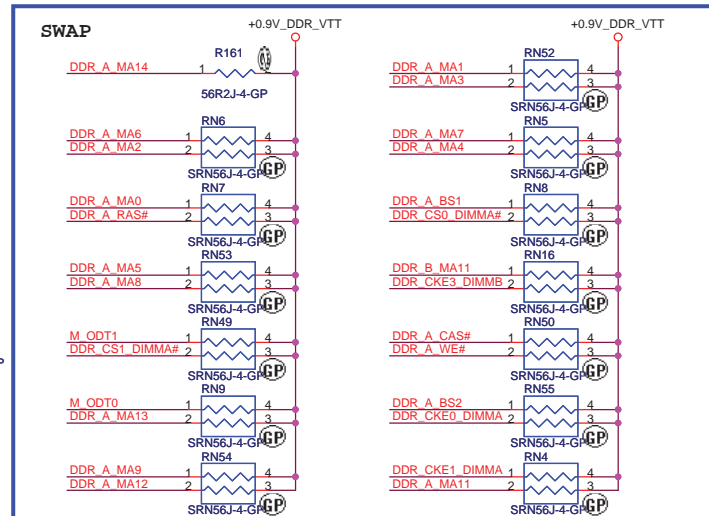
A is required to route to Top SoDIMM for AMT to function. Ch.A SoDIMM needs to be populated for Intel AMT support.



Place close to the DIMM Slot

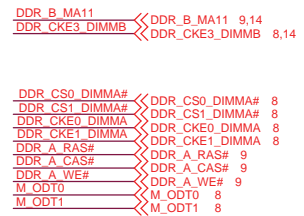


Place use One Capacitor close to every Two pull-up Resistors



M_CKE[1:0] and M_CS[1:0]# pull-up Resistors close DIMM Slot 1300 mil (MAX)

Others pull-up Resistors close DIMM Slot 750 mil (MAX)



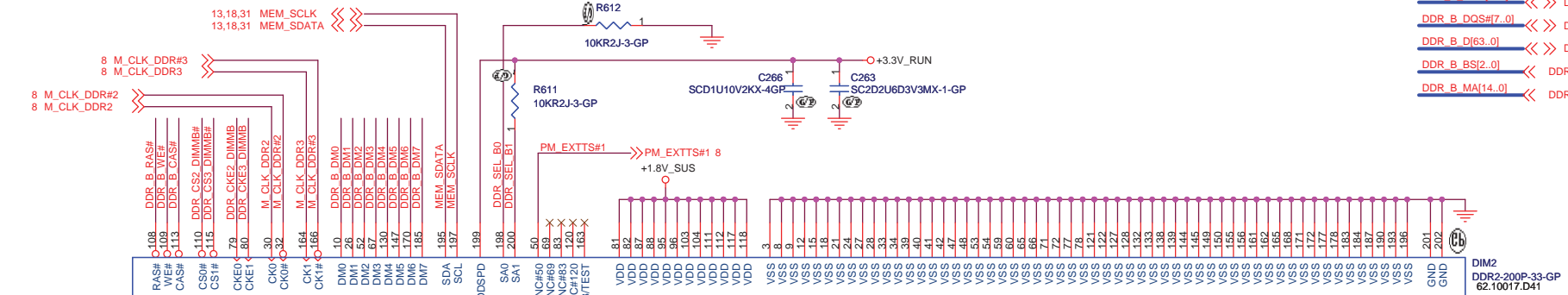
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR2-SODIMM1**

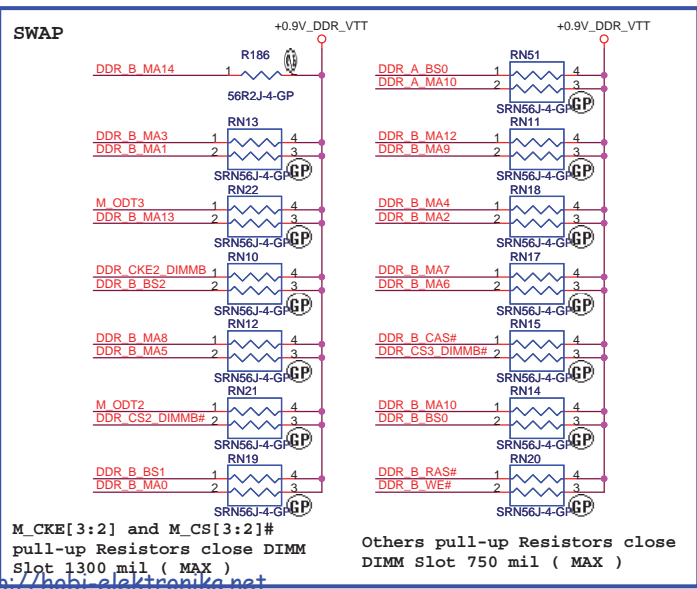
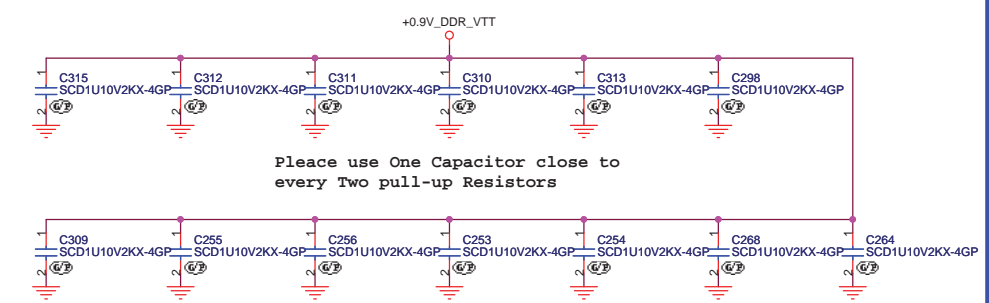
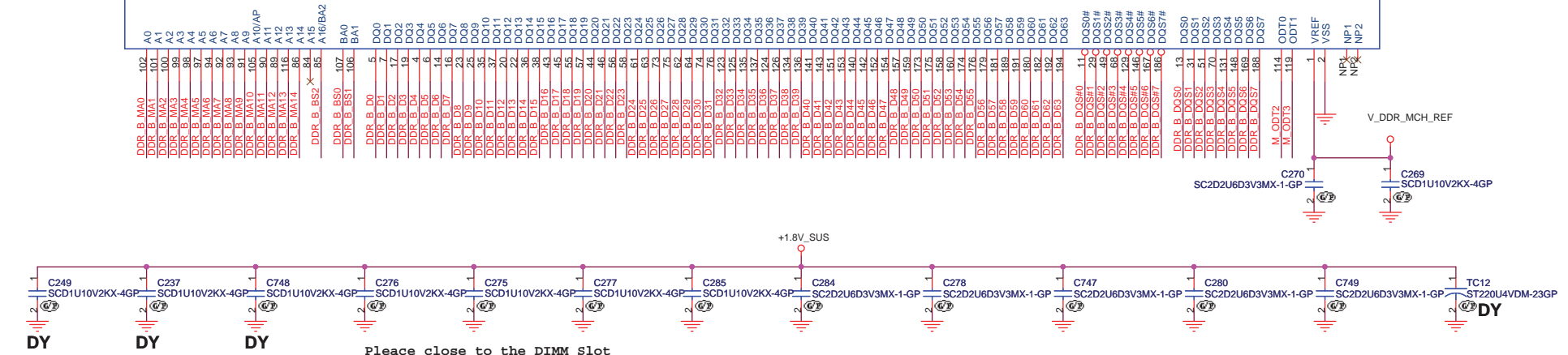
Size: A3	Document Number: Siberia	Rev: A00
Date: Monday, July 16, 2007	Sheet: 13 of 50	

M_CLK_DDR3 and M_CLK_DDR#3
can map to Row/Rank 2



- DDR_B_DM[7..0] <<> DDR_B_DM[7..0] 9
- DDR_B_DQS[7..0] <<> DDR_B_DQS[7..0] 9
- DDR_B_DQS#[7..0] <<> DDR_B_DQS#[7..0] 9
- DDR_B_D[63..0] <<> DDR_B_D[63..0] 9
- DDR_B_BS[2..0] <<> DDR_B_BS[2..0] 9
- DDR_B_MA[14..0] <<> DDR_B_MA[14..0] 9,13

REVERSE TYPE High 11mm



SWAP

DDR B MA14 <<> DDR A BS0 9,13

DDR B MA3 <<> DDR A MA10

DDR B MA2 <<> DDR A MA9

DDR B MA1 <<> DDR A MA8

M_ODT3 <<> DDR A BS0 9,13

DDR B MA13 <<> DDR A MA10

DDR CKE2_DIMMB# <<> DDR A BS0 9,13

DDR B BS2 <<> DDR A MA10

DDR B MA8 <<> DDR A MA9

DDR B MA5 <<> DDR A MA8

M_ODT2 <<> DDR A BS0 9,13

DDR CS2_DIMMB# <<> DDR A BS0 9,13

DDR B BS1 <<> DDR A MA10

DDR B MA0 <<> DDR A MA9

DDR B BS0 <<> DDR A BS0 9,13

DDR B MA10 <<> DDR A MA10

DDR B BS0 <<> DDR A BS0 9,13

DDR B RAS# <<> DDR A BS0 9,13

DDR B WE# <<> DDR A BS0 9,13

DDR CS2_DIMMB# <<> DDR A BS0 9,13

DDR CS3_DIMMB# <<> DDR A BS0 9,13

DDR CKE2_DIMMB# <<> DDR A BS0 9,13

DDR CKE3_DIMMB# <<> DDR A BS0 9,13

DDR B_RAS# <<> DDR A BS0 9,13

DDR B_CAS# <<> DDR A BS0 9,13

DDR B_WE# <<> DDR A BS0 9,13

M_ODT2 <<> DDR A BS0 9,13

M_ODT3 <<> DDR A BS0 9,13

Wistron Corporation

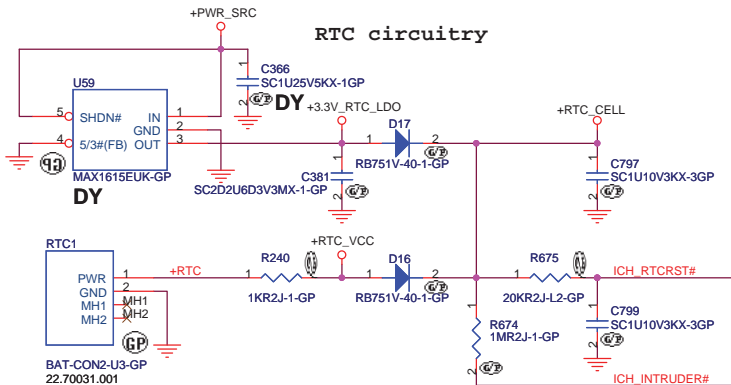
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

DDR2-SODIMM2

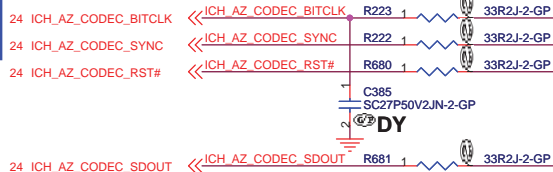
Siberia

Rev A00

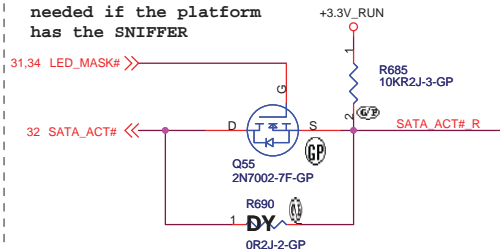
RTC circuitry



Place all series terms close to ICH8 except for SDIN input lines, which should be close to source.

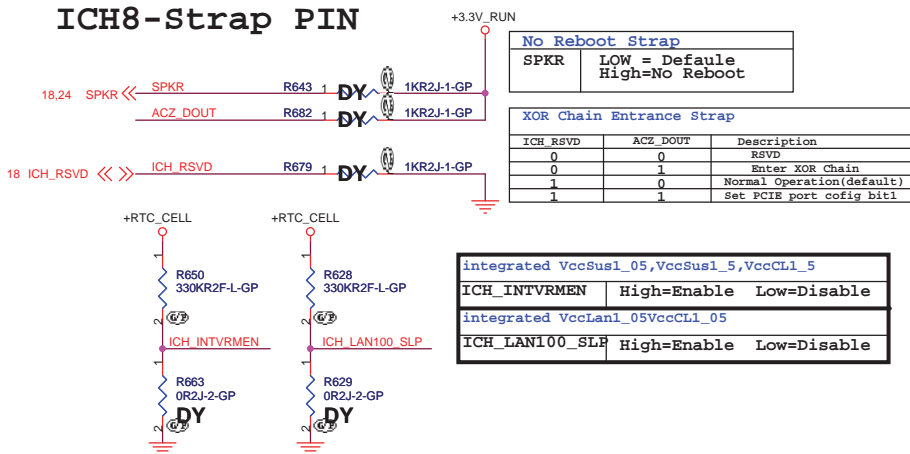


This circuit is only needed if the platform has the SNIFFER



Distance between the ICH8-M and cap on the "P" signal should be identical distance between the ICH8-M and cap on the "N" signal for same pair.

ICH8-Strap PIN



No Reboot Strap
SPKR LOW = Default
High = No Reboot

XOR Chain Entrance Strap

ICH_RSVD	ACZ_DOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

integrated VccSus1_05,VccSus1_5,VccCL1_5	
ICH_INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
ICH_LAN100_SLP	High=Enable Low=Disable

CL=12.5pF
Freq. Tolerance:±10ppm

RTC

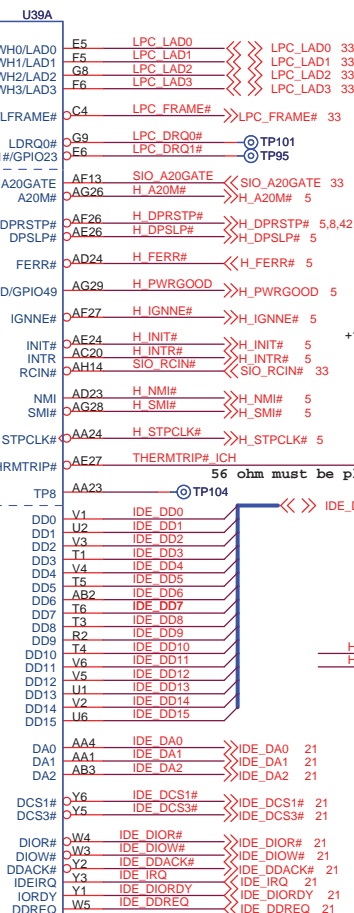
LAN/GLAN

CPU

IHDA

SATA

IDE



<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
ICH8M-RTC/IDE/LPC/DHI (1/4)		
Size	Document Number	Rev
A3	Siberia	A00
Date:	Monday, July 16, 2007	Sheet 16 of 50

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	MiniCard WPAN
LANE4	Express Card
LANE5	PPU Card
LANE6	Giba Bit LOM

Capacitors close to ICH8-M

U39E 2 OF 6

The diagram shows the connection of various capacitors to the ICH8-M chip. The components are organized into four main functional blocks, each with a dashed border and a label:

- PCI-Express**: Contains connections for PCI Express lanes (PCIE RX1- to PCIE TX6+), DMI MTX/IRX signals (N0 to N6), and DMI MRX/ITX signals (N0 to N6).
- Direct Media Interface**: Contains connections for DMI MTX/IRX signals (N0 to N6), DMI MRX/ITX signals (N0 to N6), and DMI ZCOMP/IRCOMP signals (Y24).
- SPI**: Contains connections for SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, and SPI_MISO.
- USB**: Contains connections for USB_OC0_1#, USB_OC2_3#, and USB_OC4#.

Capacitors are labeled with values such as 15R2J-GP, 15R2J-1, 15R2J-2, 15R2J-3, 15R2J-4, 15R2J-5, 15R2J-6, 15R2J-7, 15R2J-8, 15R2J-9, 15R2J-10, 15R2J-11, 15R2J-12, 15R2J-13, 15R2J-14, 15R2J-15, 15R2J-16, 15R2J-17, 15R2J-18, 15R2J-19, 15R2J-20, 15R2J-21, 15R2J-22, 15R2J-23, 15R2J-24, 15R2J-25, 15R2J-26, 15R2J-27, 15R2J-28, 15R2J-29, 15R2J-30, 15R2J-31, 15R2J-32, 15R2J-33, 15R2J-34, 15R2J-35, 15R2J-36, 15R2J-37, 15R2J-38, 15R2J-39, 15R2J-40, 15R2J-41, 15R2J-42, 15R2J-43, 15R2J-44, 15R2J-45, 15R2J-46, 15R2J-47, 15R2J-48, 15R2J-49, 15R2J-50, 15R2J-51, 15R2J-52, 15R2J-53, 15R2J-54, 15R2J-55, 15R2J-56, 15R2J-57, 15R2J-58, 15R2J-59, 15R2J-60, 15R2J-61, 15R2J-62, 15R2J-63, 15R2J-64, 15R2J-65, 15R2J-66, 15R2J-67, 15R2J-68, 15R2J-69, 15R2J-70, 15R2J-71, 15R2J-72, 15R2J-73, 15R2J-74, 15R2J-75, 15R2J-76, 15R2J-77, 15R2J-78, 15R2J-79, 15R2J-80, 15R2J-81, 15R2J-82, 15R2J-83, 15R2J-84, 15R2J-85, 15R2J-86, 15R2J-87, 15R2J-88, 15R2J-89, 15R2J-90, 15R2J-91, 15R2J-92, 15R2J-93, 15R2J-94, 15R2J-95, 15R2J-96, 15R2J-97, 15R2J-98, 15R2J-99, 15R2J-100, 15R2J-101, 15R2J-102, 15R2J-103, 15R2J-104, 15R2J-105, 15R2J-106, 15R2J-107, 15R2J-108, 15R2J-109, 15R2J-110, 15R2J-111, 15R2J-112, 15R2J-113, 15R2J-114, 15R2J-115, 15R2J-116, 15R2J-117, 15R2J-118, 15R2J-119, 15R2J-120, 15R2J-121, 15R2J-122, 15R2J-123, 15R2J-124, 15R2J-125, 15R2J-126, 15R2J-127, 15R2J-128, 15R2J-129, 15R2J-130, 15R2J-131, 15R2J-132, 15R2J-133, 15R2J-134, 15R2J-135, 15R2J-136, 15R2J-137, 15R2J-138, 15R2J-139, 15R2J-140, 15R2J-141, 15R2J-142, 15R2J-143, 15R2J-144, 15R2J-145, 15R2J-146, 15R2J-147, 15R2J-148, 15R2J-149, 15R2J-150, 15R2J-151, 15R2J-152, 15R2J-153, 15R2J-154, 15R2J-155, 15R2J-156, 15R2J-157, 15R2J-158, 15R2J-159, 15R2J-160, 15R2J-161, 15R2J-162, 15R2J-163, 15R2J-164, 15R2J-165, 15R2J-166, 15R2J-167, 15R2J-168, 15R2J-169, 15R2J-170, 15R2J-171, 15R2J-172, 15R2J-173, 15R2J-174, 15R2J-175, 15R2J-176, 15R2J-177, 15R2J-178, 15R2J-179, 15R2J-180, 15R2J-181, 15R2J-182, 15R2J-183, 15R2J-184, 15R2J-185, 15R2J-186, 15R2J-187, 15R2J-188, 15R2J-189, 15R2J-190, 15R2J-191, 15R2J-192, 15R2J-193, 15R2J-194, 15R2J-195, 15R2J-196, 15R2J-197, 15R2J-198, 15R2J-199, 15R2J-200, 15R2J-201, 15R2J-202, 15R2J-203, 15R2J-204, 15R2J-205, 15R2J-206, 15R2J-207, 15R2J-208, 15R2J-209, 15R2J-210, 15R2J-211, 15R2J-212, 15R2J-213, 15R2J-214, 15R2J-215, 15R2J-216, 15R2J-217, 15R2J-218, 15R2J-219, 15R2J-220, 15R2J-221, 15R2J-222, 15R2J-223, 15R2J-224, 15R2J-225, 15R2J-226, 15R2J-227, 15R2J-228, 15R2J-229, 15R2J-230, 15R2J-231, 15R2J-232, 15R2J-233, 15R2J-234, 15R2J-235, 15R2J-236, 15R2J-237, 15R2J-238, 15R2J-239, 15R2J-240, 15R2J-241, 15R2J-242, 15R2J-243, 15R2J-244, 15R2J-245, 15R2J-246, 15R2J-247, 15R2J-248, 15R2J-249, 15R2J-250, 15R2J-251, 15R2J-252, 15R2J-253, 15R2J-254, 15R2J-255, 15R2J-256, 15R2J-257, 15R2J-258, 15R2J-259, 15R2J-260, 15R2J-261, 15R2J-262, 15R2J-263, 15R2J-264, 15R2J-265, 15R2J-266, 15R2J-267, 15R2J-268, 15R2J-269, 15R2J-270, 15R2J-271, 15R2J-272, 15R2J-273, 15R2J-274, 15R2J-275, 15R2J-276, 15R2J-277, 15R2J-278, 15R2J-279, 15R2J-280, 15R2J-281, 15R2J-282, 15R2J-283, 15R2J-284, 15R2J-285, 15R2J-286, 15R2J-287, 15R2J-288, 15R2J-289, 15R2J-290, 15R2J-291, 15R2J-292, 15R2J-293, 15R2J-294, 15R2J-295, 15R2J-296, 15R2J-297, 15R2J-298, 15R2J-299, 15R2J-300, 15R2J-301, 15R2J-302, 15R2J-303, 15R2J-304, 15R2J-305, 15R2J-306, 15R2J-307, 15R2J-308, 15R2J-309, 15R2J-310, 15R2J-311, 15R2J-312, 15R2J-313, 15R2J-314, 15R2J-315, 15R2J-316, 15R2J-317, 15R2J-318, 15R2J-319, 15R2J-320, 15R2J-321, 15R2J-322, 15R2J-323, 15R2J-324, 15R2J-325, 15R2J-326, 15R2J-327, 15R2J-328, 15R2J-329, 15R2J-330, 15R2J-331, 15R2J-332, 15R2J-333, 15R2J-334, 15R2J-335, 15R2J-336, 15R2J-337, 15R2J-338, 15R2J-339, 15R2J-340, 15R2J-341, 15R2J-342, 15R2J-343, 15R2J-344, 15R2J-345, 15R2J-346, 15R2J-347, 15R2J-348, 15R2J-349, 15R2J-350, 15R2J-351, 15R2J-352, 15R2J-353, 15R2J-354,

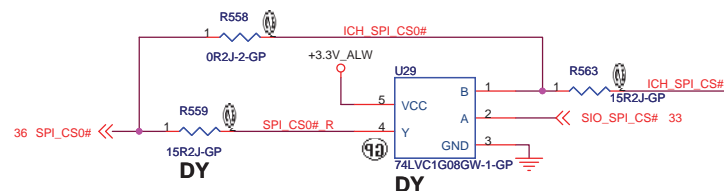
ICH8-Strap PIN

18 PCI_GNT#0 << PCI_GNT#0 R598 1 1KR2J-1-GP
 ICH_SPI_CS1# R595 1 DY 1KR2J-1-GP
 18 PCI_GNT#3 << PCI_GNT#3 R596 1 DY 1KR2J-1-GP

Pin configuration diagram for the RP4 module. The module is shown with pins 1 through 10. Pin 1 is USB_OC5#, pin 2 is USB_OC9#, pin 3 is USB_OC6#, pin 4 is USB_OC7#, pin 5 is +3.3V_SUS, pin 6 is USB_OC0 1#, pin 7 is USB_OC4#, pin 8 is USB_OC8#, pin 9 is USB_OC2 3#, and pin 10 is +3.3V_SUS. The module is labeled RP4 and SRN10KH 3-GP.

ICH

USB0	Ext Left Side
USB1	Ext Back
USB2	Ext Right Side (Top)
USB3	Ext Right Side (Bottom)
USB4	3rd mini card
USB5	Camera
USB6	Express Card
USB7	BT
USB8	Gaming LCD
USB9	WWAN



DELL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

ICH8M-PCIE/USB/SPI/DMI (2/4)

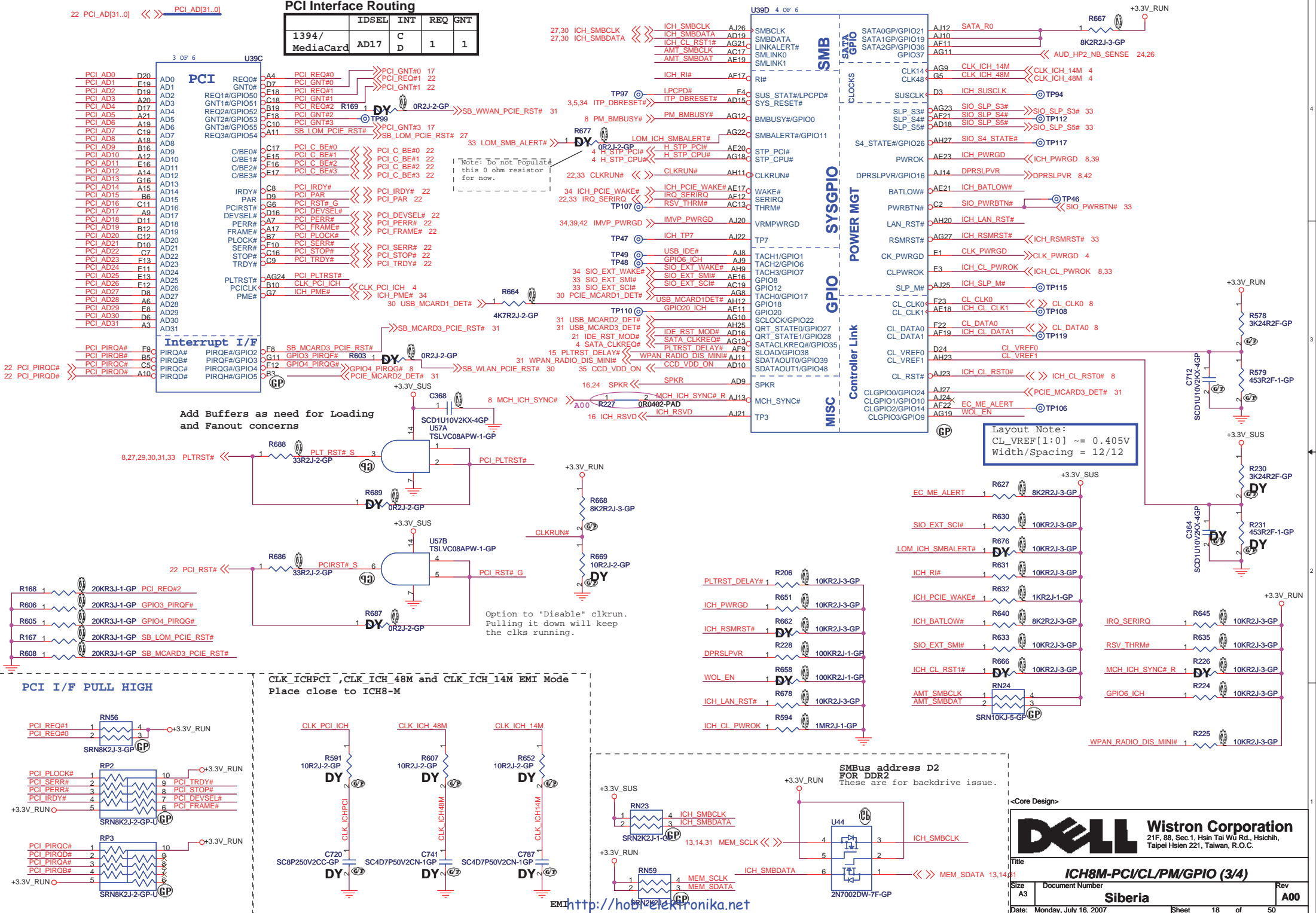
Siberia

Rev	
A00	

Sheet 17 of 50

PCI Interface Routing

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD17	C D	1	1



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

ICH8M-PCI/CL/PM/GPIO (3/4)

Size A3 Document Number Siberia Rev A00

Date: Monday, July 16, 2007 Sheet 18 of 50

SSID = THERMAL

REM_DIODE1_N and REM_DIODE1_P
routing Trace width and Spacing
use 10 / 10 mil

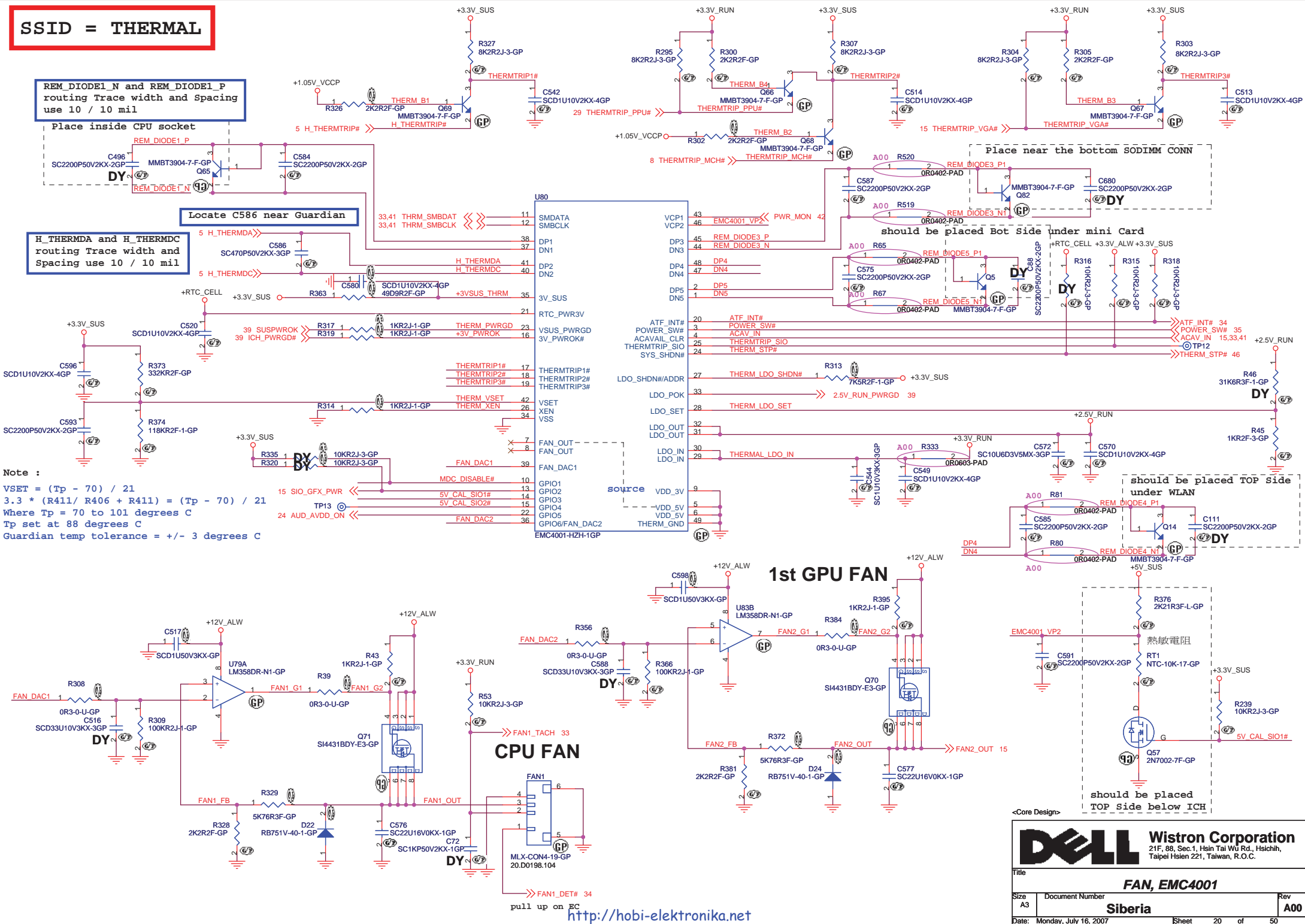
Place inside CPU socket

Locate C586 near Guardian

H_THERMDA and H_THERMDC
routing Trace width and
Spacing use 10 / 10 mil

Note :

$VSET = (T_p - 70) / 21$
 $3.3 * (R411 / R406 + R411) = (T_p - 70) / 21$
 Where $T_p = 70$ to 101 degrees C
 T_p set at 88 degrees C
 Guardian temp tolerance = +/- 3 degrees C



<http://hobi-elektronika.net>

<Core Design>

DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

File _____

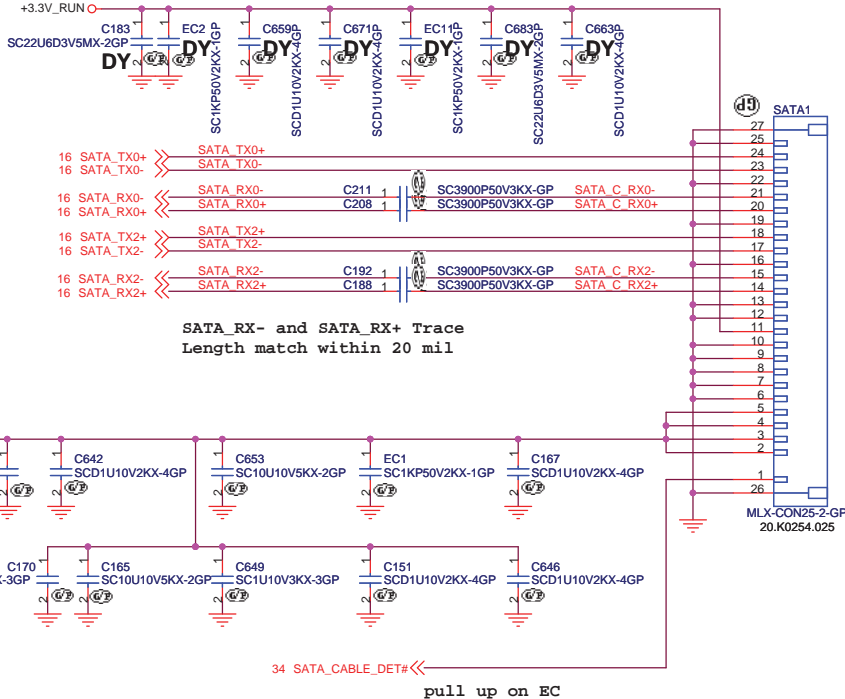
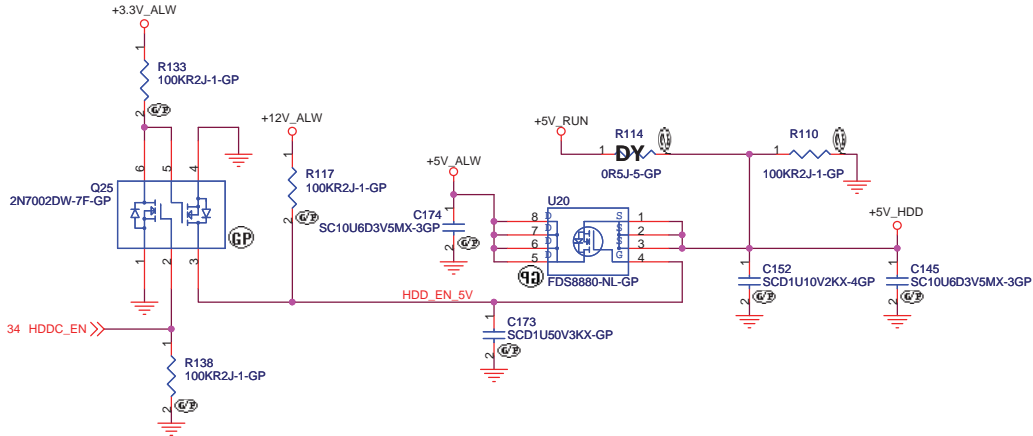
Size A3 Document Number _____ Rev A00

Date: Monday, July 16, 2007 Sheet 20 of 50

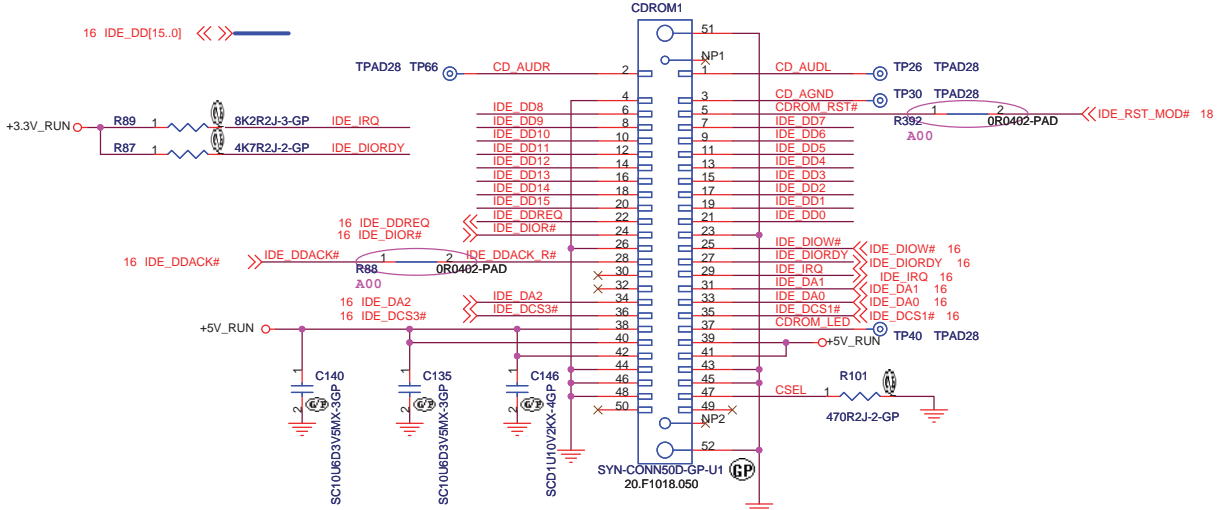
FAN, EMC4001
Siberia

SSID = IDE & SATA

SATA HDD Connector



ODD Connector

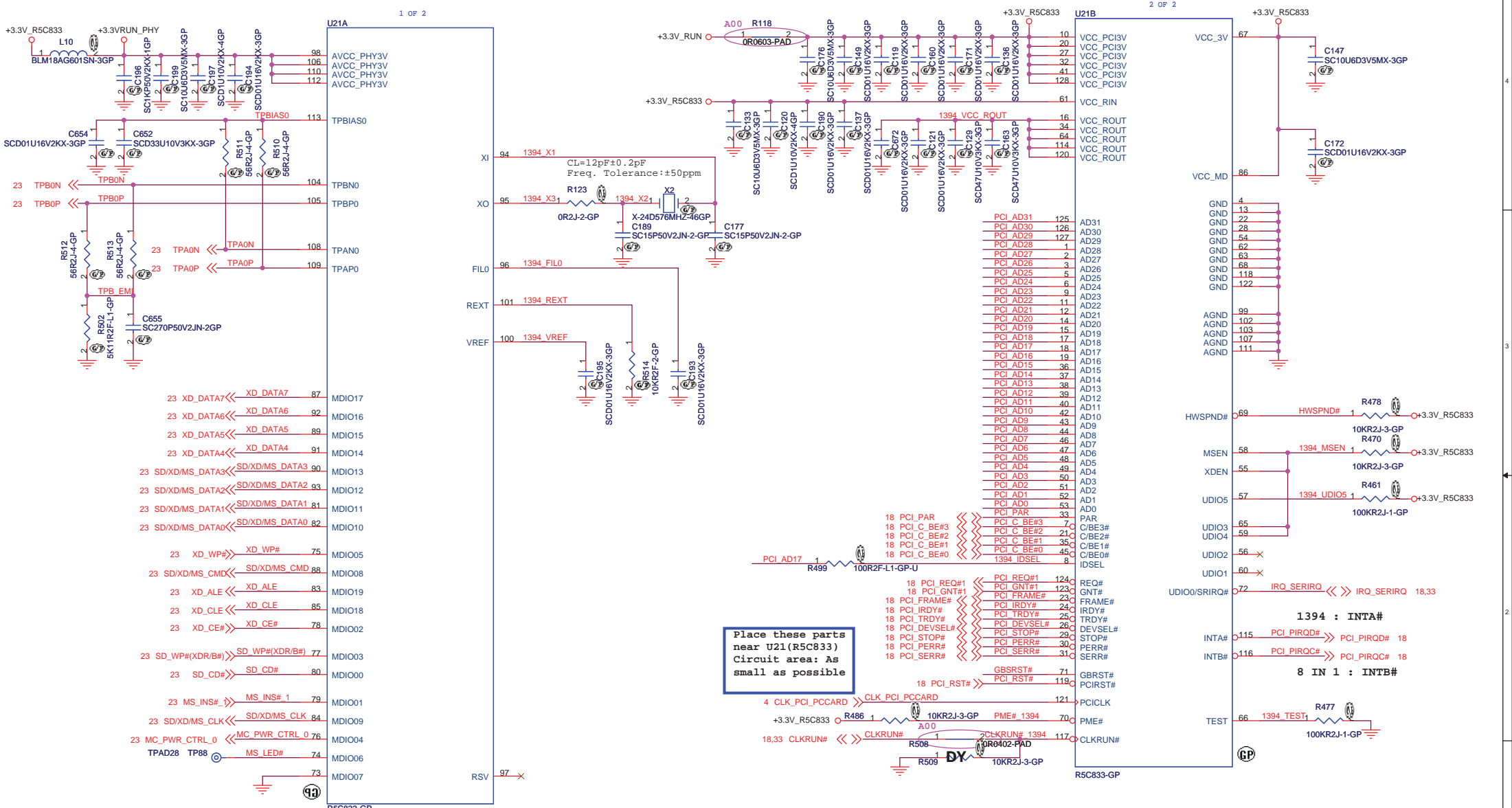


<Core Design>

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD&ODD**

Size A3	Document Number	Rev A00
Date: Monday, July 16, 2007	Sheet 21 of 50	



We use the R5C832 in X00 for R5C833 not ready.

SSID = 1394



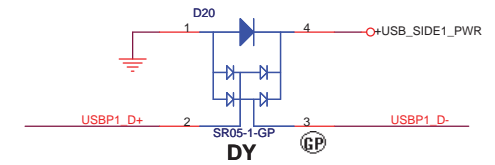
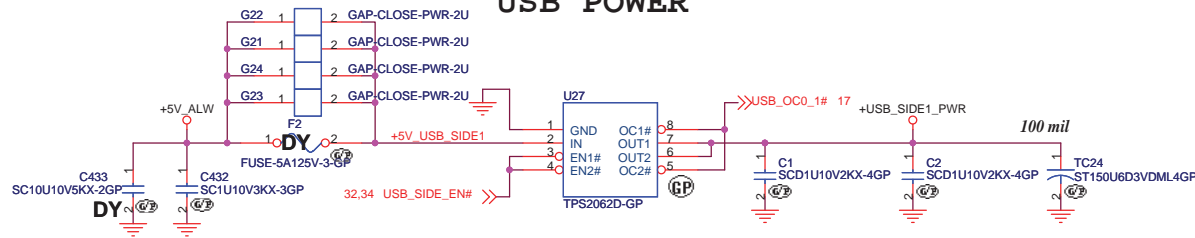
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

1394 - R5C833

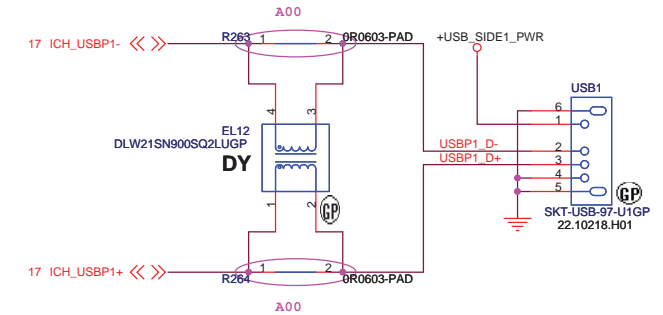
Size A3 Document Number Siberia Rev A00

Date: Monday, July 16, 2007 Sheet 22 of 50

USB POWER

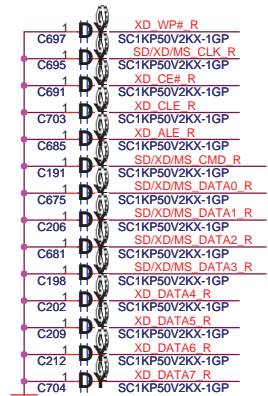
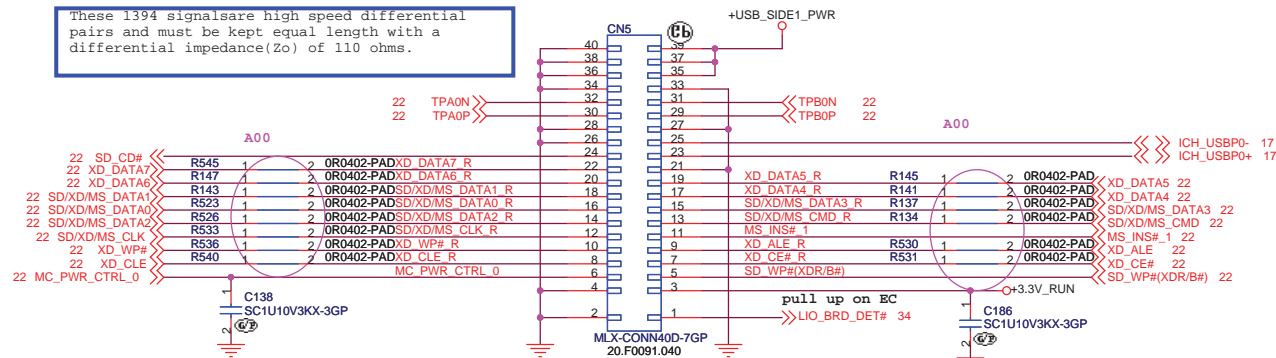


Place ESD diodes as close to the connector as possible.



I/O board conn. (1394/7 IN 1/USB)

These 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance (Z_0) of 110 ohms.

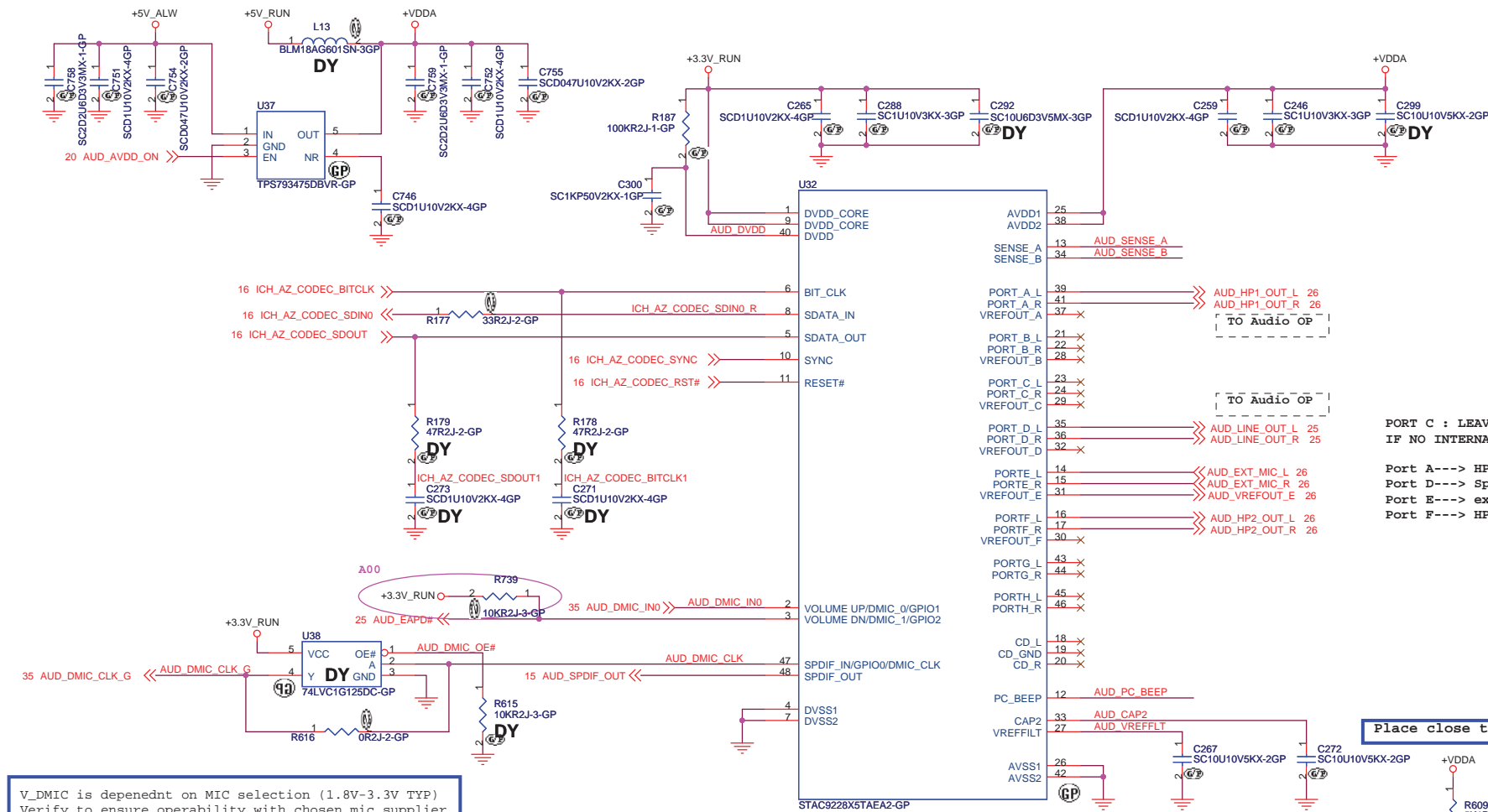


<Core Design>

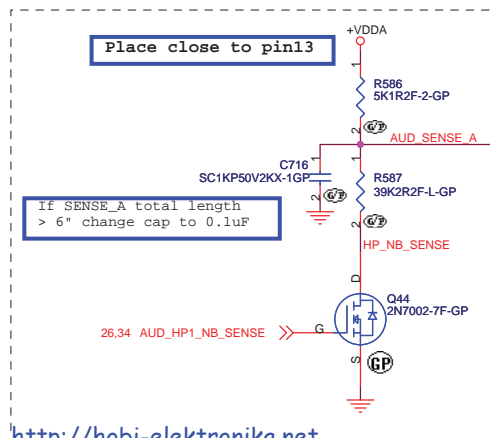
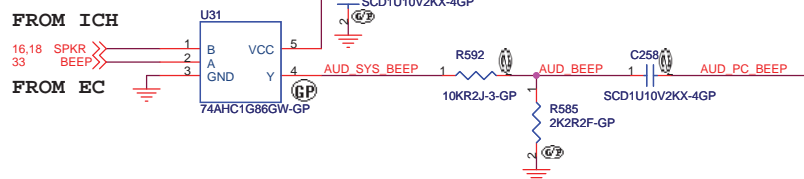
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
I/O board (1394/7 IN 1/USB) / USB CONN.

Size A3	Document Number Siberia	Rev A00
Date: Monday, July 16, 2007	Sheet 23 of 50	



V_DMIC is depenednt on MIC selection (1.8V-3.3V TYP)
Verify to ensure operability with chosen mic supplier.
Note1: If only 1 digital mic, use AUD_DMIC_IN0.
Note2: If using 2 digital mics, also use AUD_DMIC_IN0.
This input supports 2 digital mics.
AUD_DMIC_IN1 is only used to support 4 digital mics.



If SENSE_B total length > 6" change cap to 0.1uF

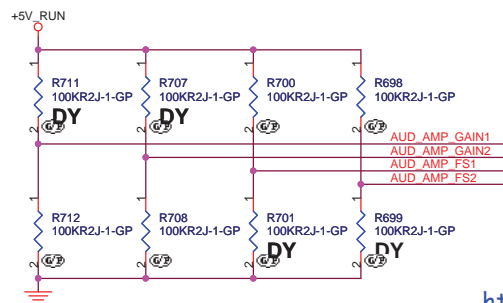
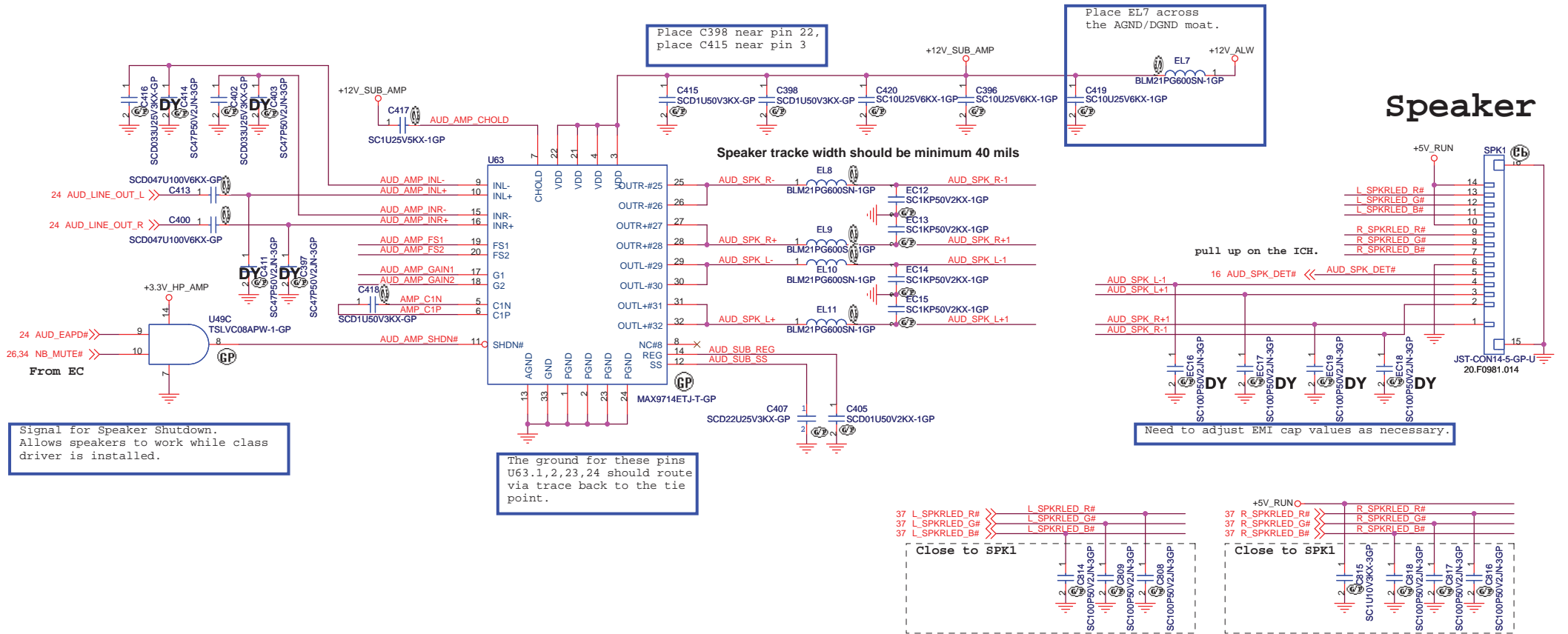
18,26 AUD_HP2_NB_SENSE > G Q54 2N7002-7F-GP Q50 2N7002-7F-GP > AUD_MIC_SWITCH 26,34

<Core Design>

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Size	Document Number	Rev
A3	Siberia	A00
Date:	Monday, July 16, 2007	Sheet 24 of 50

<http://hobi-elektronika.net>



Oscillator frequency selection

FS1	FS2	Freq KHz
0	0	335
0	1	460
1	0	236
1	1	335+/-7% (ss mode)

Voltage Gain selection

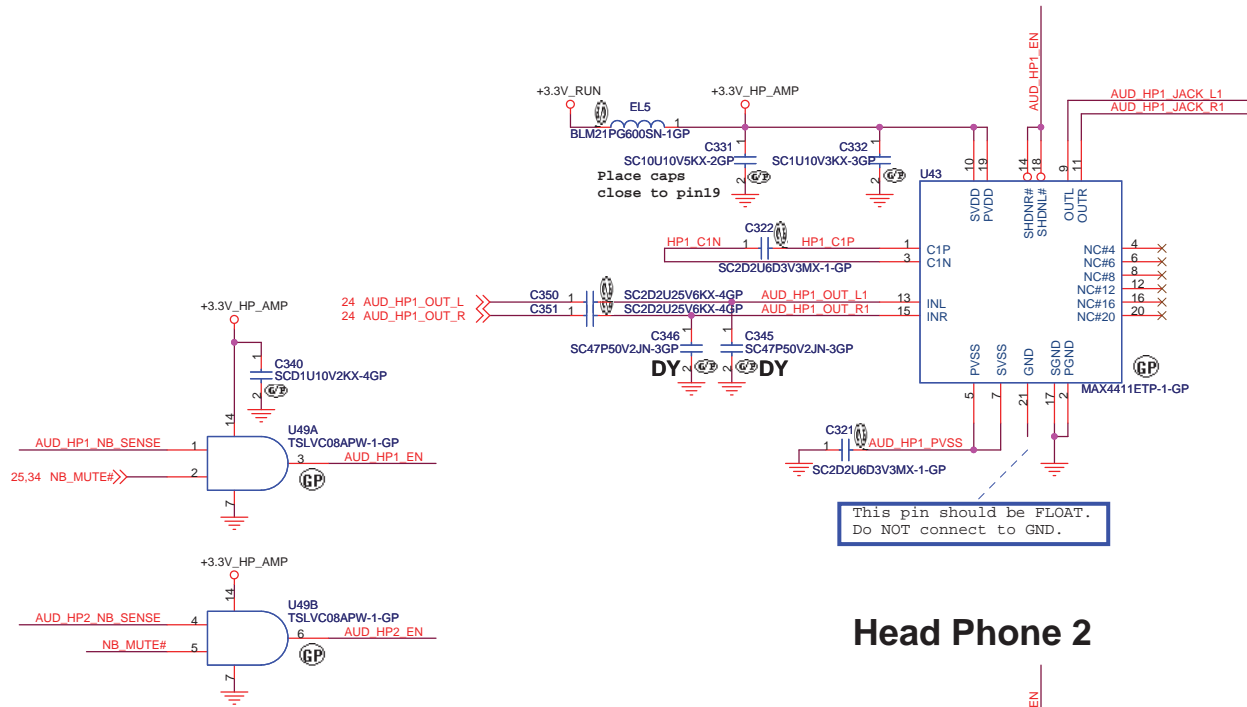
G1	G2	AV dB	Input Impedance
0	0	22.1dB	31K ohm
0	1	19.1dB	39K ohm
1	0	13dB	58K ohm
1	1	16dB	48K ohm

<Core Design>

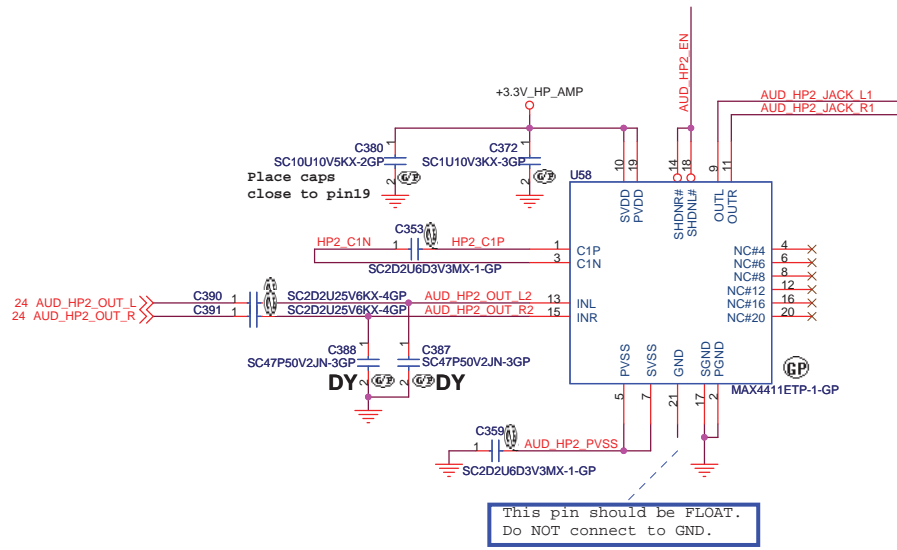
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO (2/3)**
Size: A3 Document Number: **Siberia** Rev: **A00**
Date: Monday, July 16, 2007 Sheet: 25 of 50

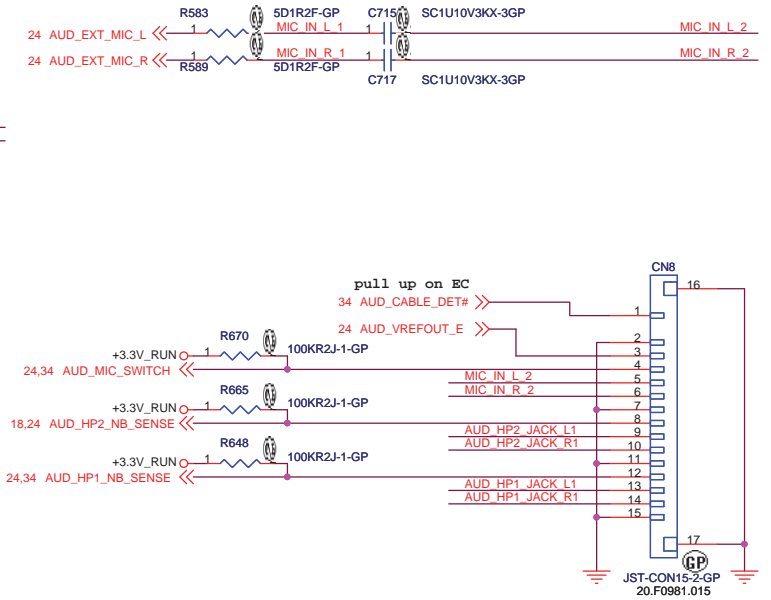
Head Phone 1



Head Phone 2



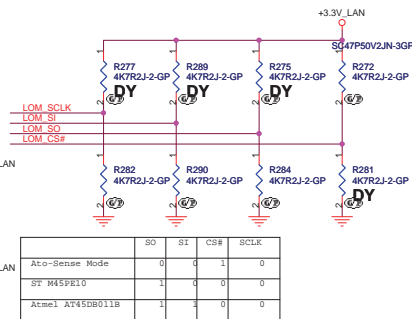
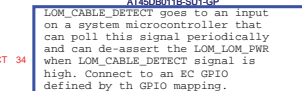
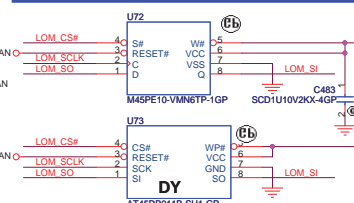
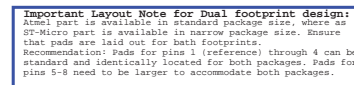
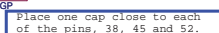
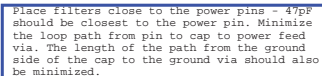
MIC



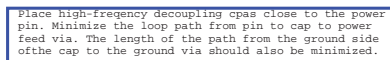
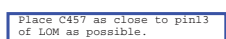
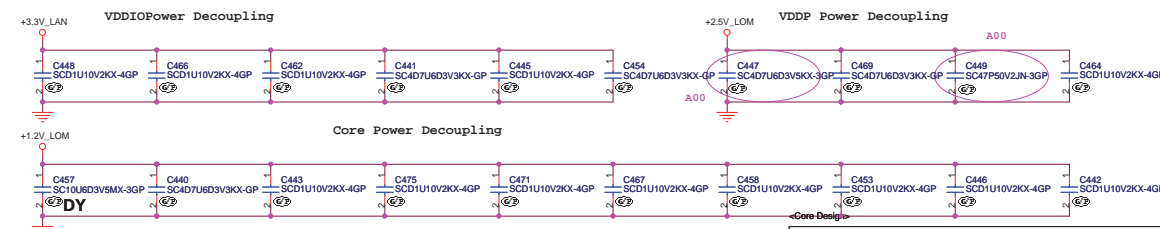
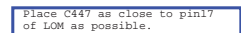
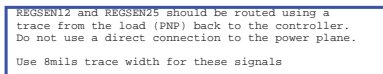
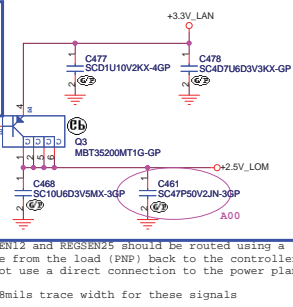
<Core Design>

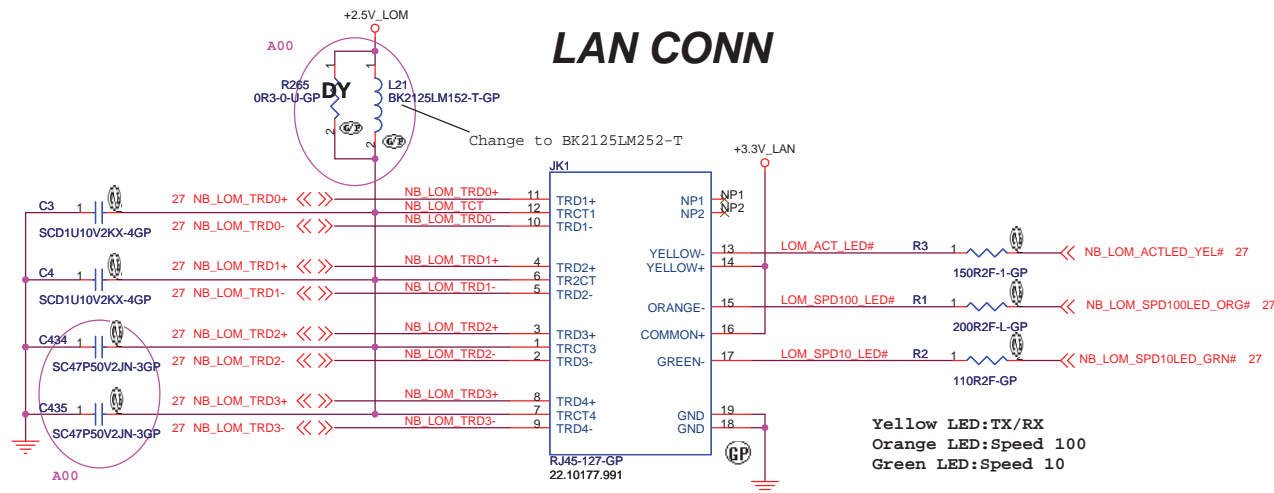
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			AUDIO (3/3)	
Size	Document Number	Rev		
A3	Siberia	A00		
Date:	Monday, July 16, 2007	Sheet	26	of 50



	SO	SI	CS#	SCLK
Ato-Sense Mode	0	0	1	0
ST M45PE10	1	0	0	0
Atmel AT45DB011B	1	1	0	0





1. Route as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. Pairs must be equal lengths.
5. 4mil trace width, 7mil separation.
6. 30mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

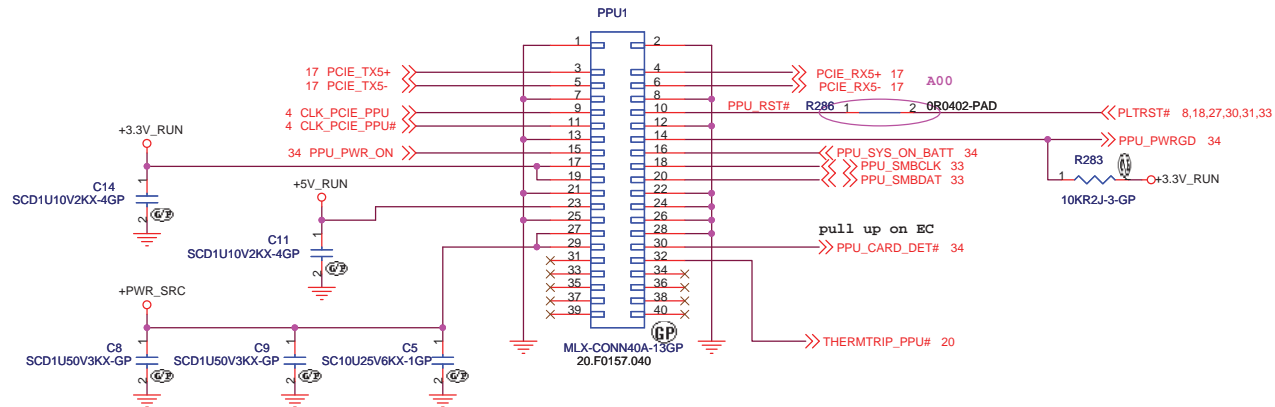
The blowout from the LAN magnetics to the RJ45 connector maintaining the distance between the two to be within 1 inch.

<Core Design>

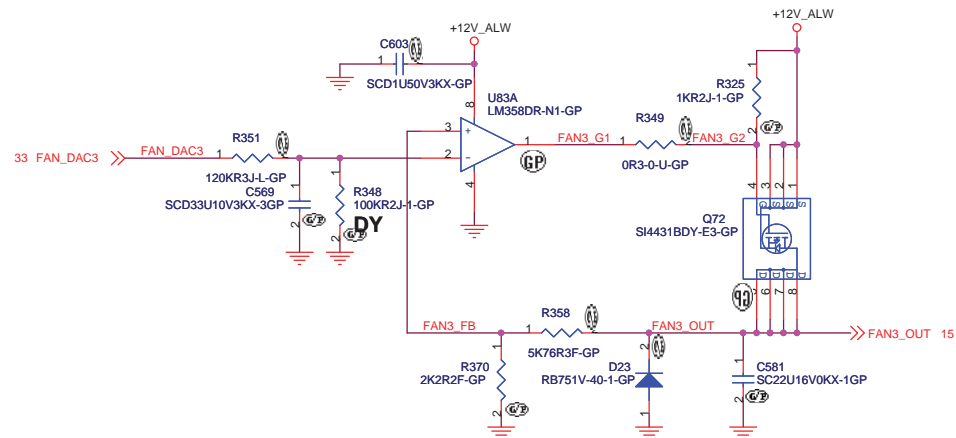


Title			LAN Connector	
Size	Document Number	Siberia		Rev
A3				A00
Date:	Monday, July 16, 2007	Sheet	28 of 50	

PPU connector



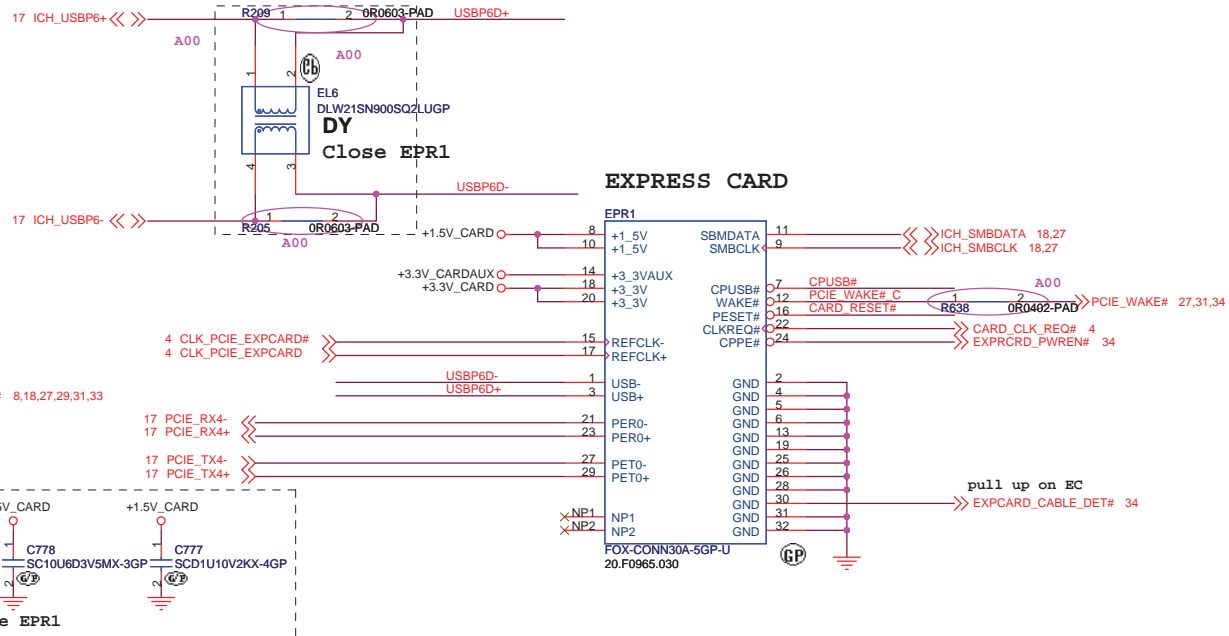
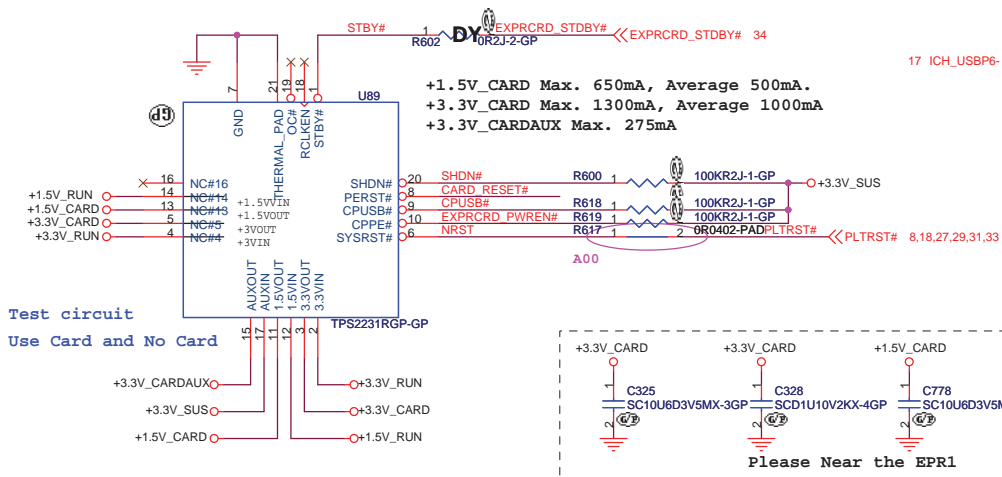
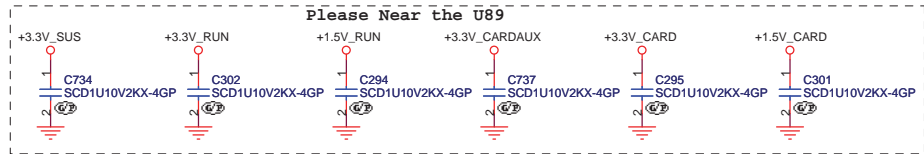
2nd GPU FAN



<Core Design>

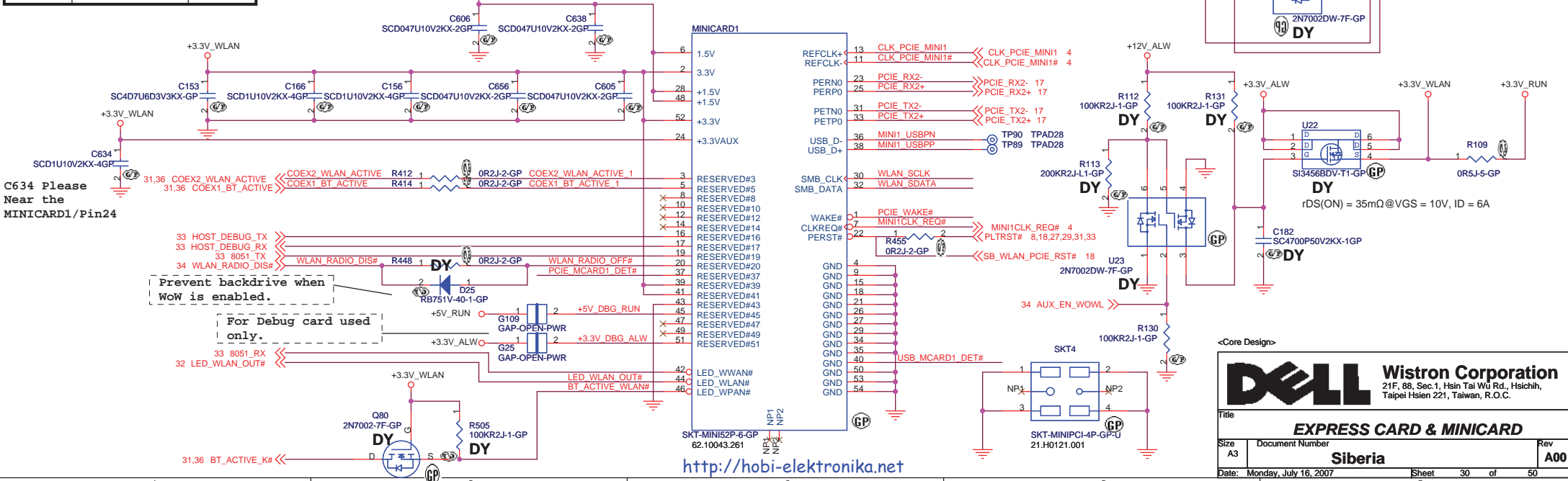
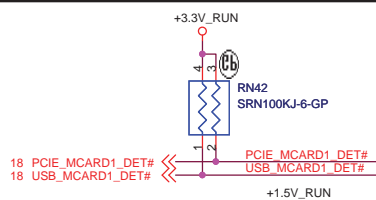


Title			
PPU CONN. / 2rd GPU FAN			
Size	Document Number		Rev
A3	Siberia		A00
Date:	Monday, July 16, 2007	Sheet	29 of 50



DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81



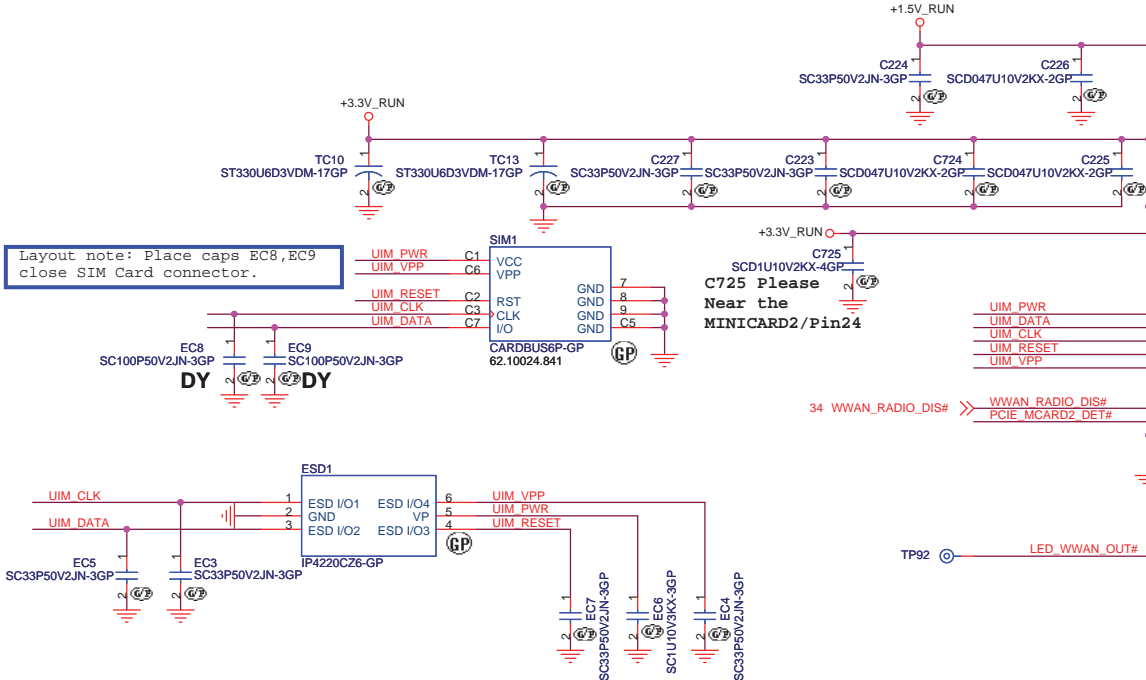
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

EXPRESS CARD & MINICARD

Size A3 Document Number Siberia Rev A00

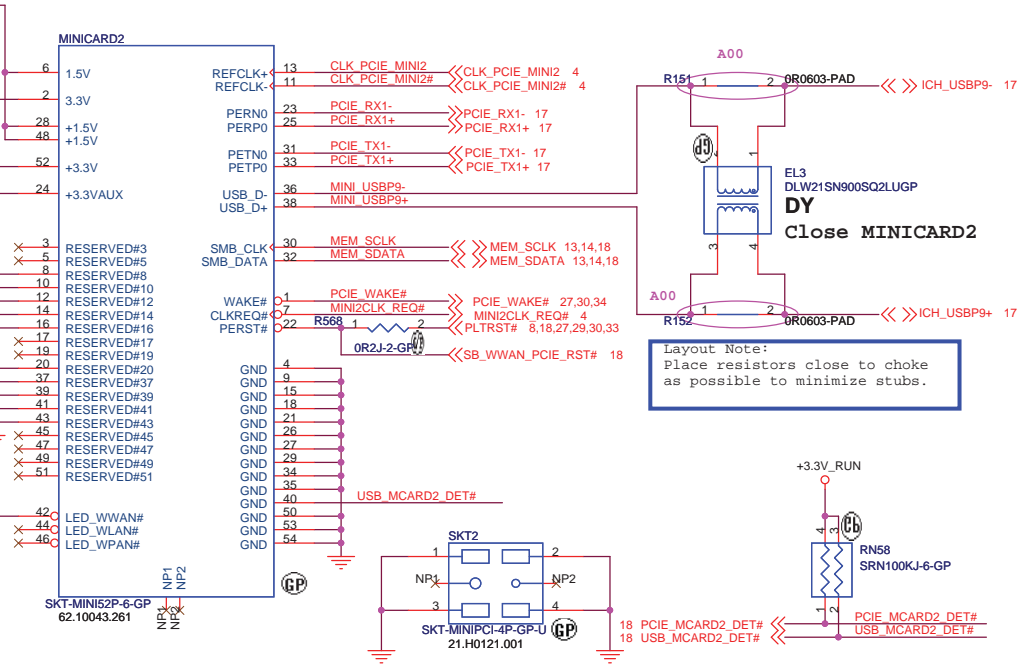
Date: Monday, July 16, 2007 Sheet 30 of 50

Layout note: Place caps EC8, EC9 close SIM Card connector.



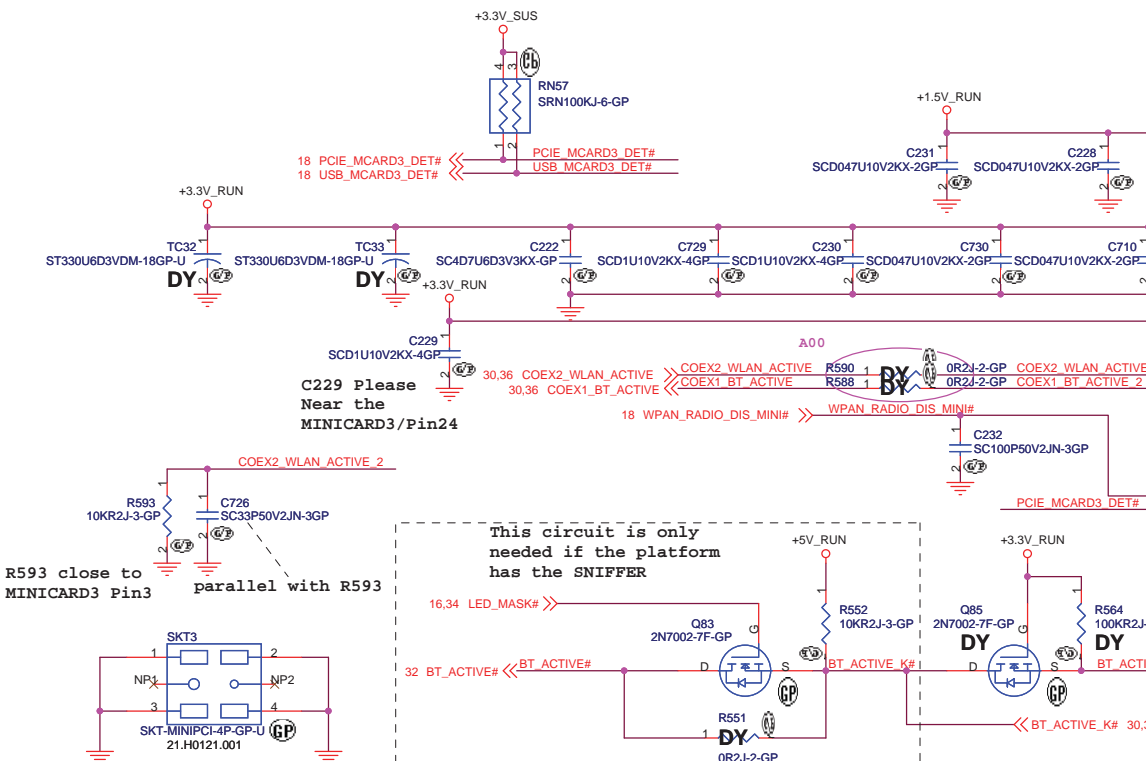
Layout note: Place caps EC3-EC7 close Mini Card connector.

MiniCard WWAN connector

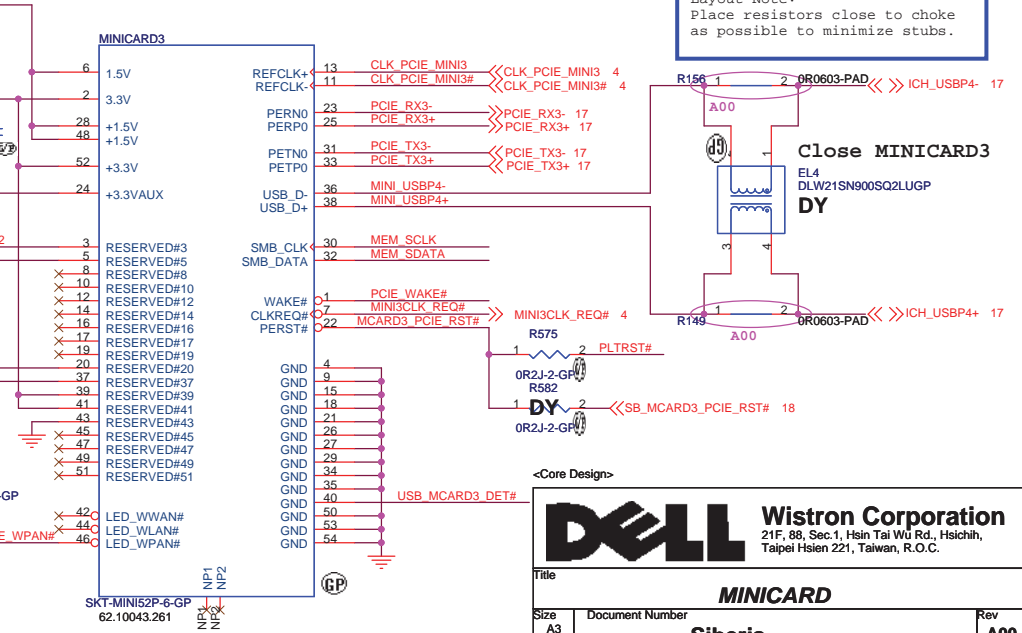


Layout Note: Place resistors close to choke as possible to minimize stubs.

MiniCard WPAN connector



Layout Note: Place resistors close to choke as possible to minimize stubs.



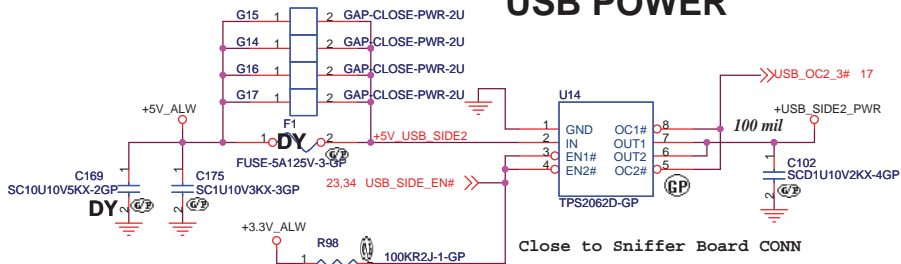
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

MINICARD

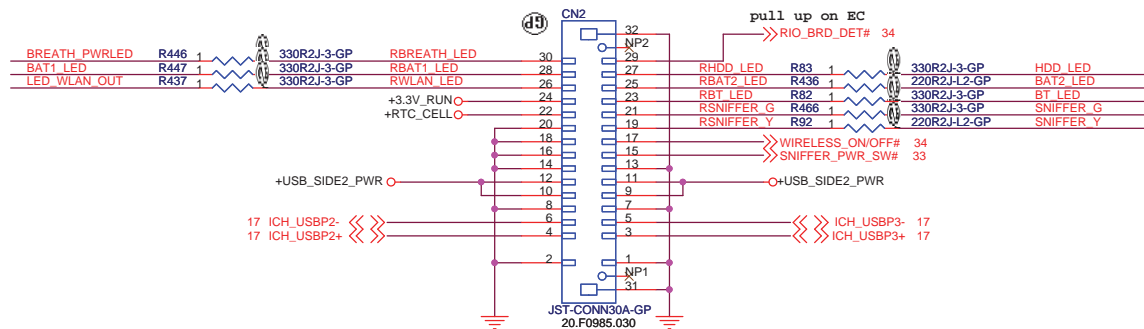
Size A3 Document Number Siberia Rev A00

Date: Monday, July 16, 2007 Sheet 31 of 50

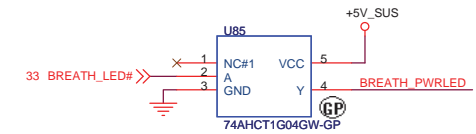
USB POWER



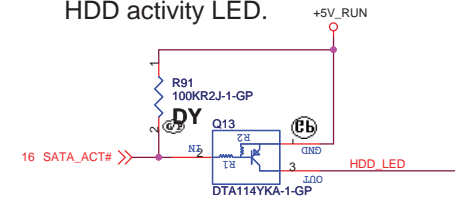
Sniffer board for USB, Indicator LEDs, Sniffer Switch conn.



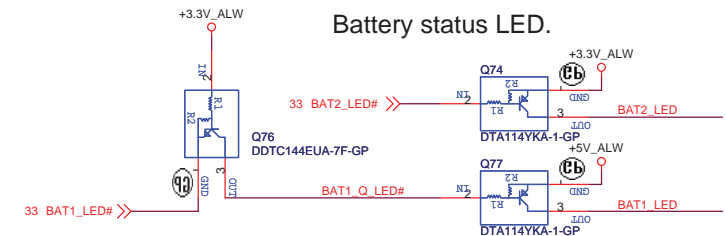
Power & Suspend LED.



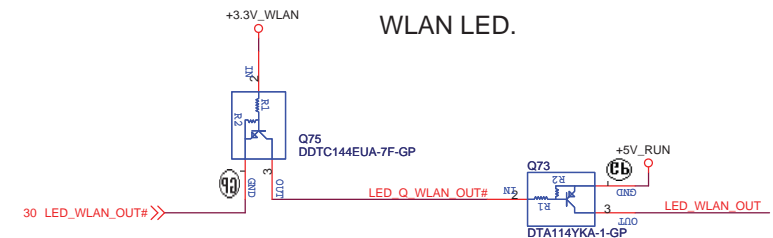
HDD activity LED.



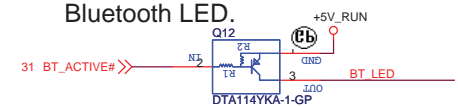
Battery status LED.



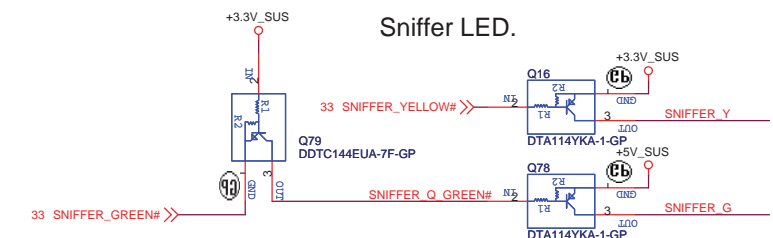
WLAN LED.



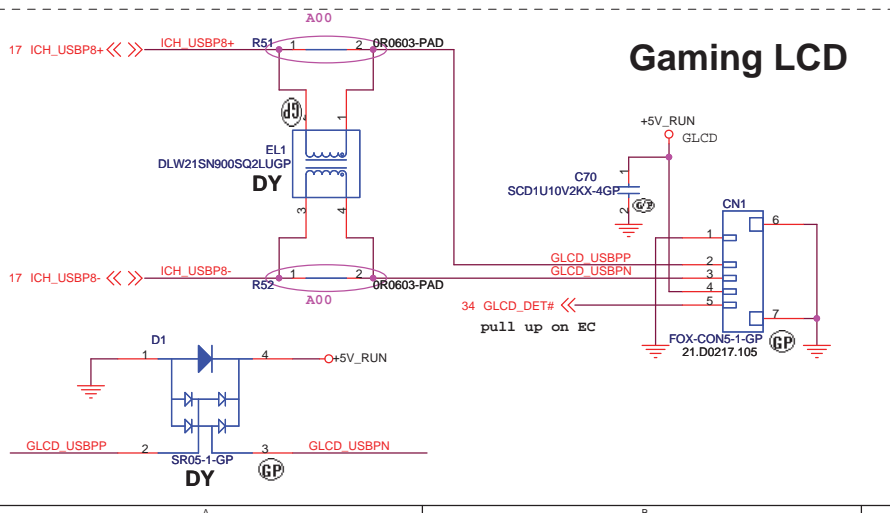
Bluetooth LED.



Sniffer LED.



Gaming LCD



<http://hobi-elektronika.net>

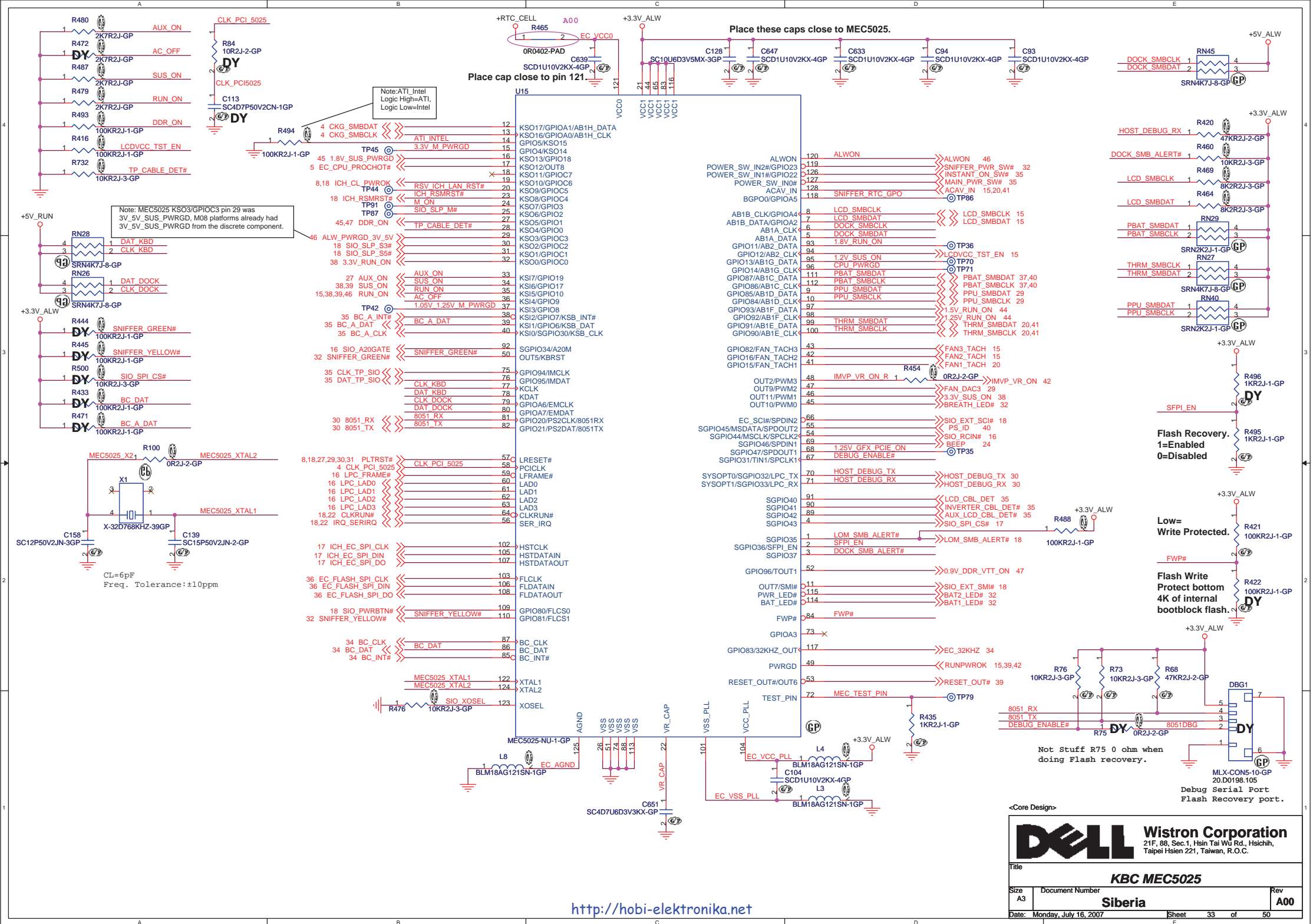
<Core Design>

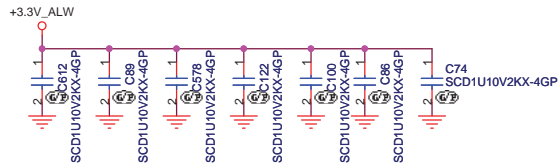
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **Sniffer board (USB/Status LEDs) / Gaming LCD**

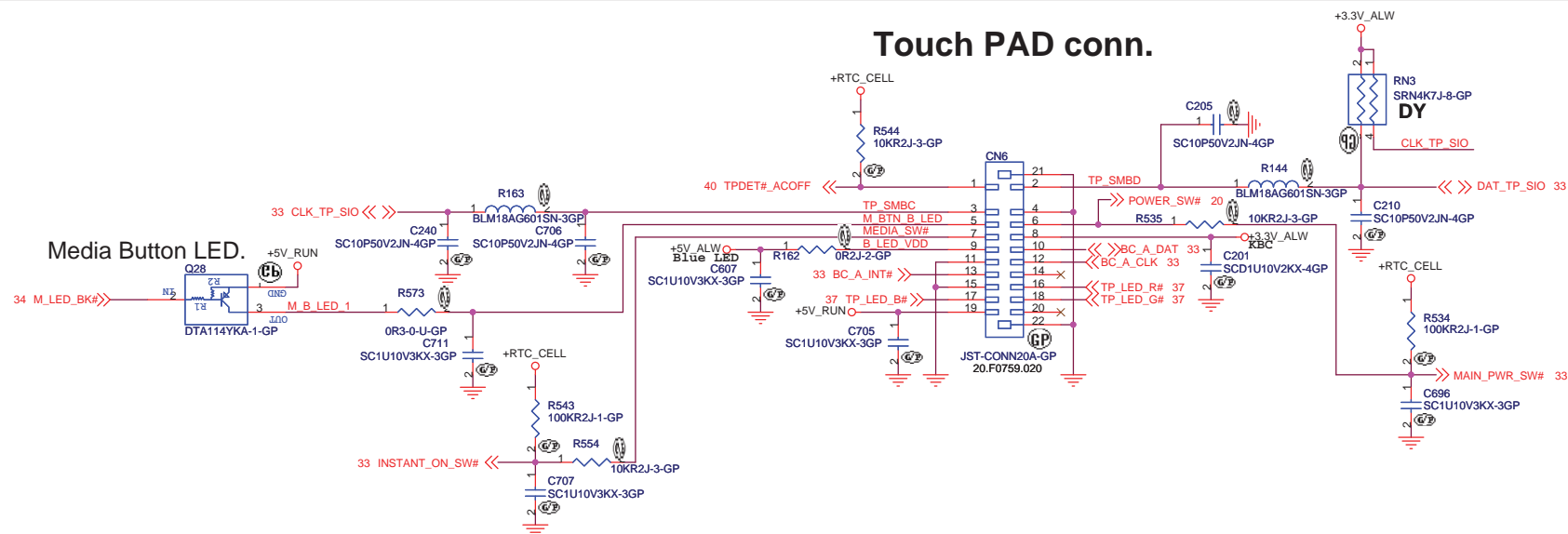
Size A3 Document Number **Siberia** Rev **A00**

Date: Monday, July 16, 2007 Sheet 32 of 50

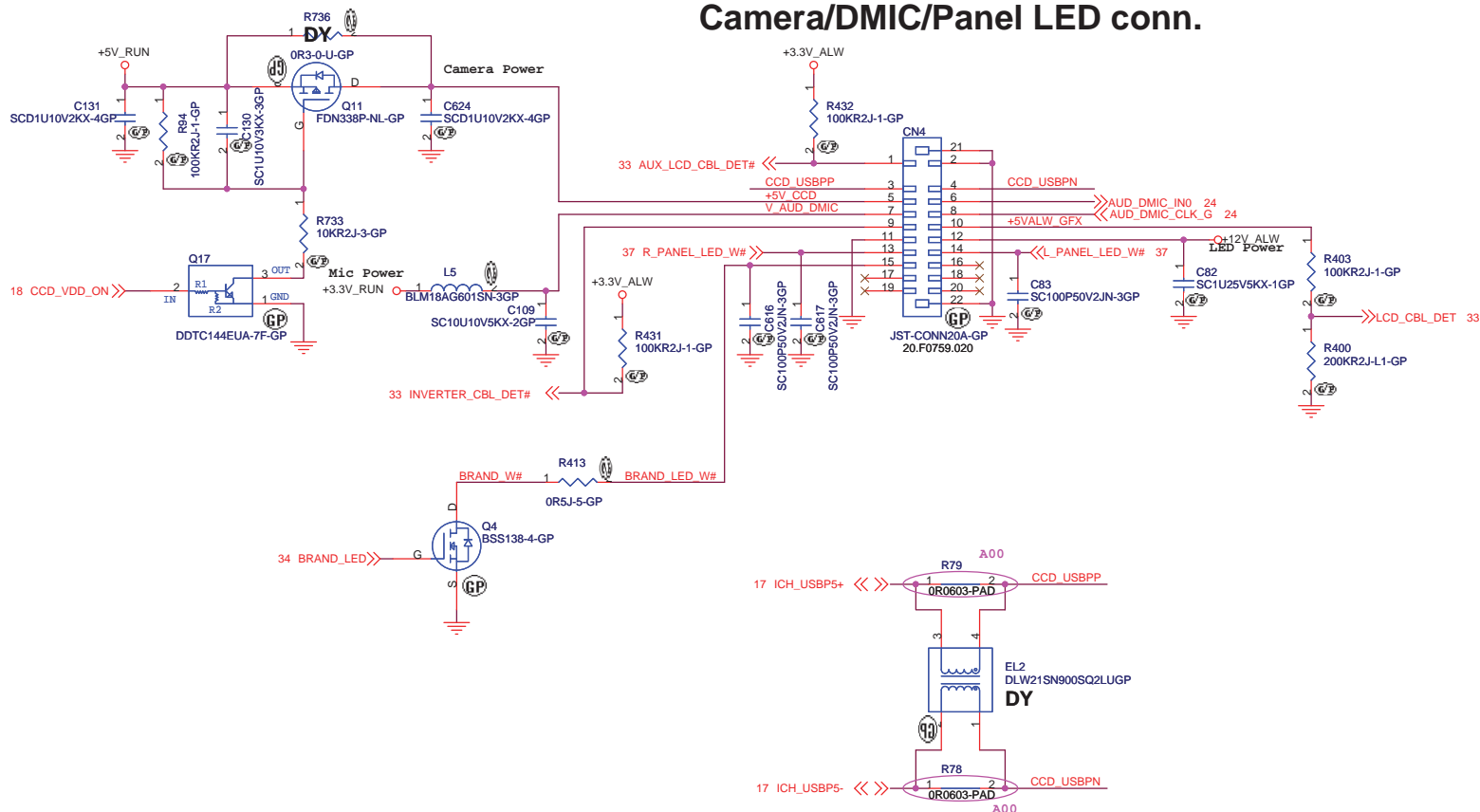




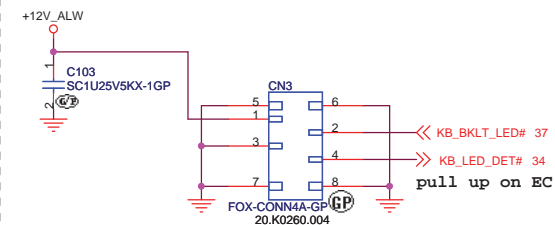
Touch PAD conn.


$$\overline{r_{DS(ON)}} = 115\text{m}\Omega @ \overline{V_{GS}} = -4.5\text{V}, \overline{I_D} = -1.6\text{A}$$

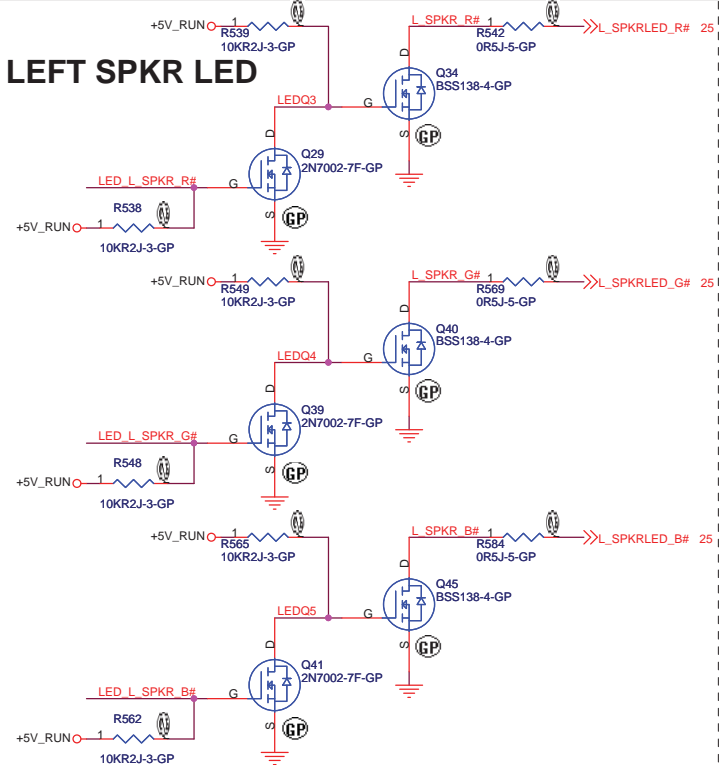
Camera/DMIC/Panel LED conn.



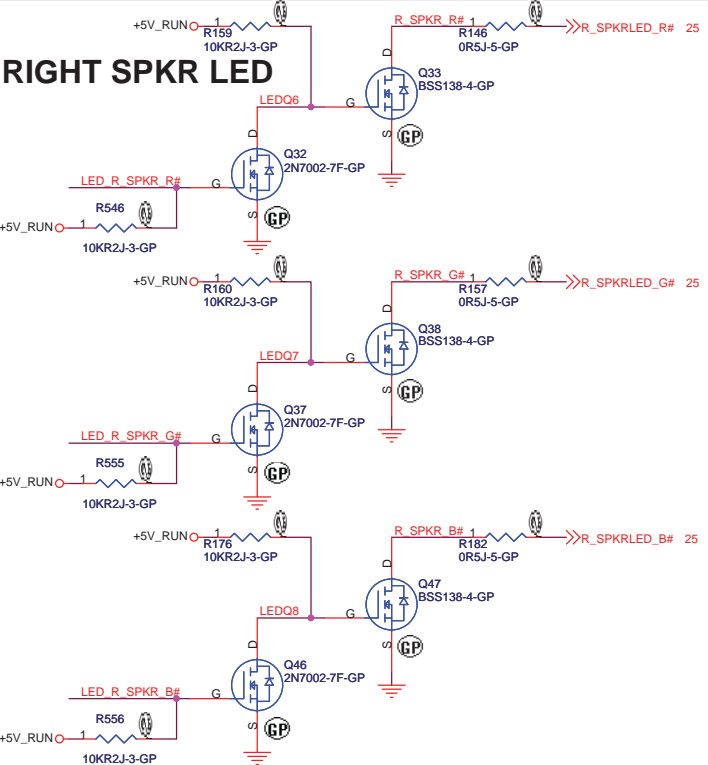
KB BKLT LED



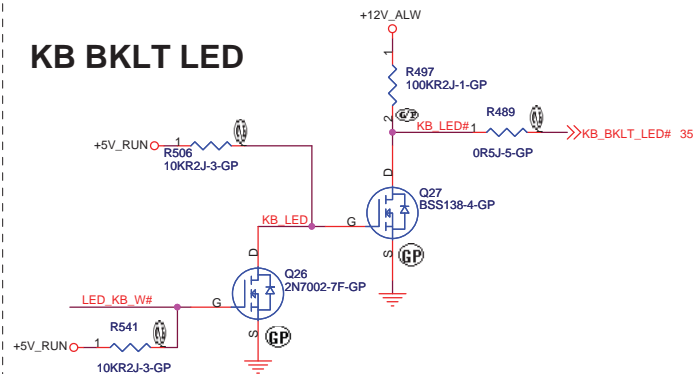
LEFT SPKR LED



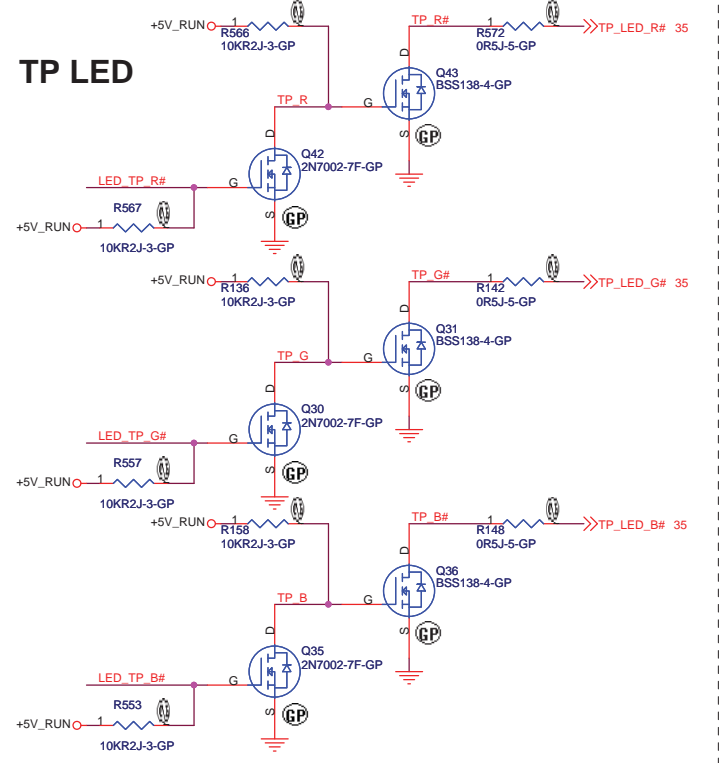
RIGHT SPKR LED



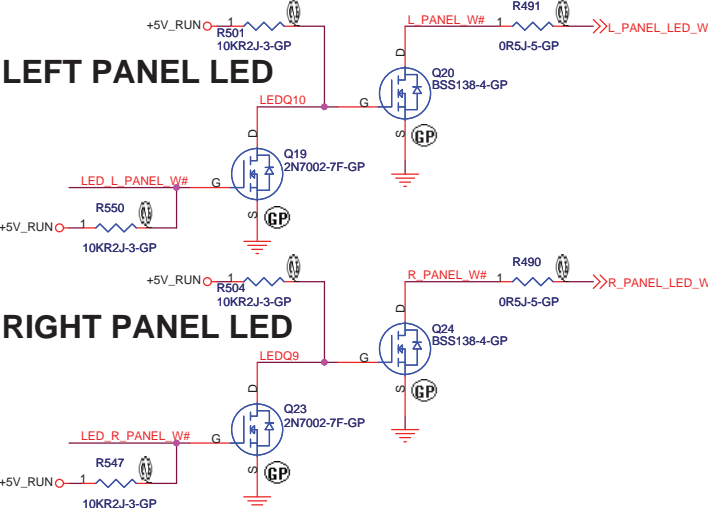
KB BKLT LED



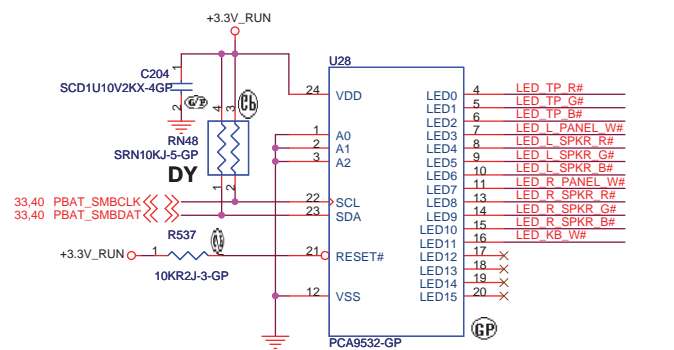
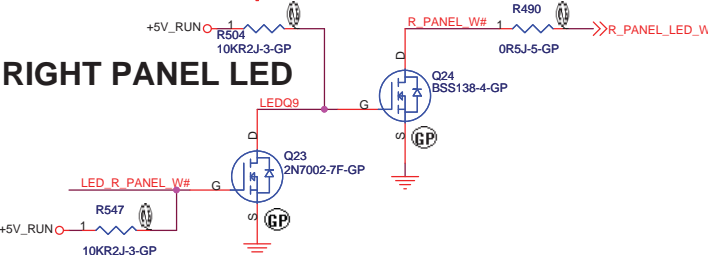
TP LED

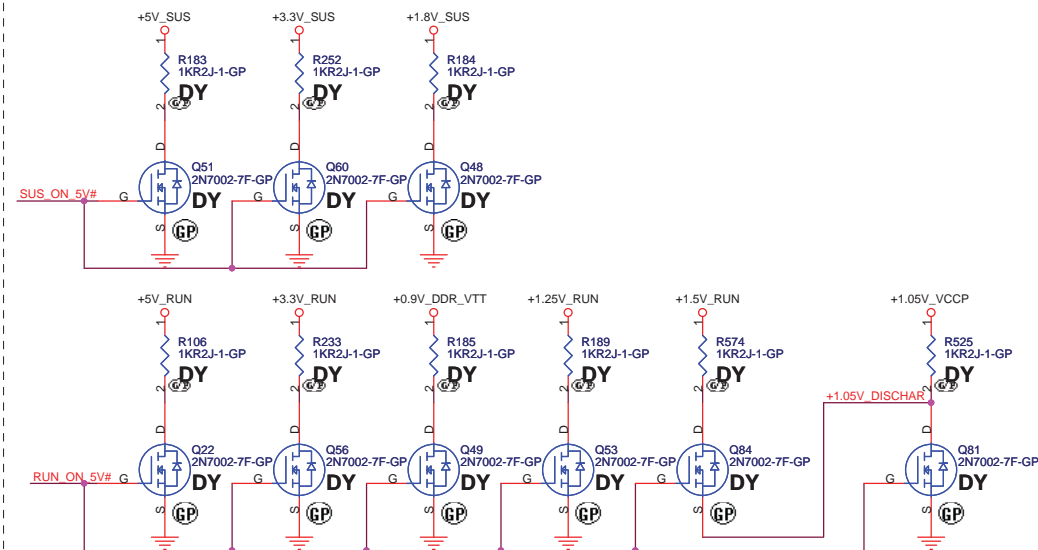
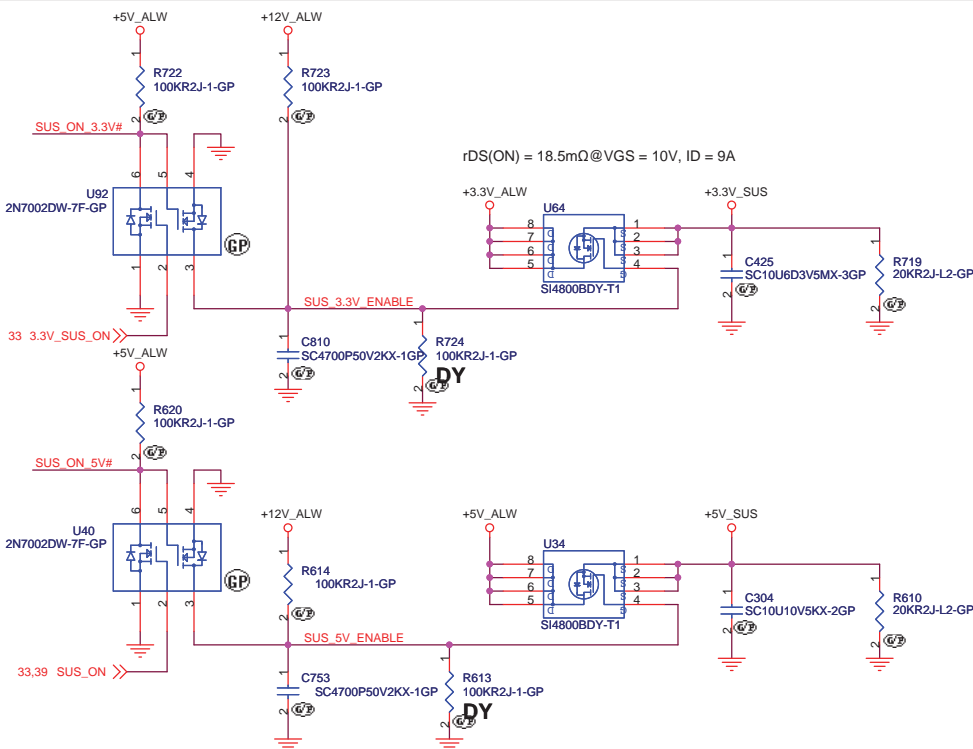
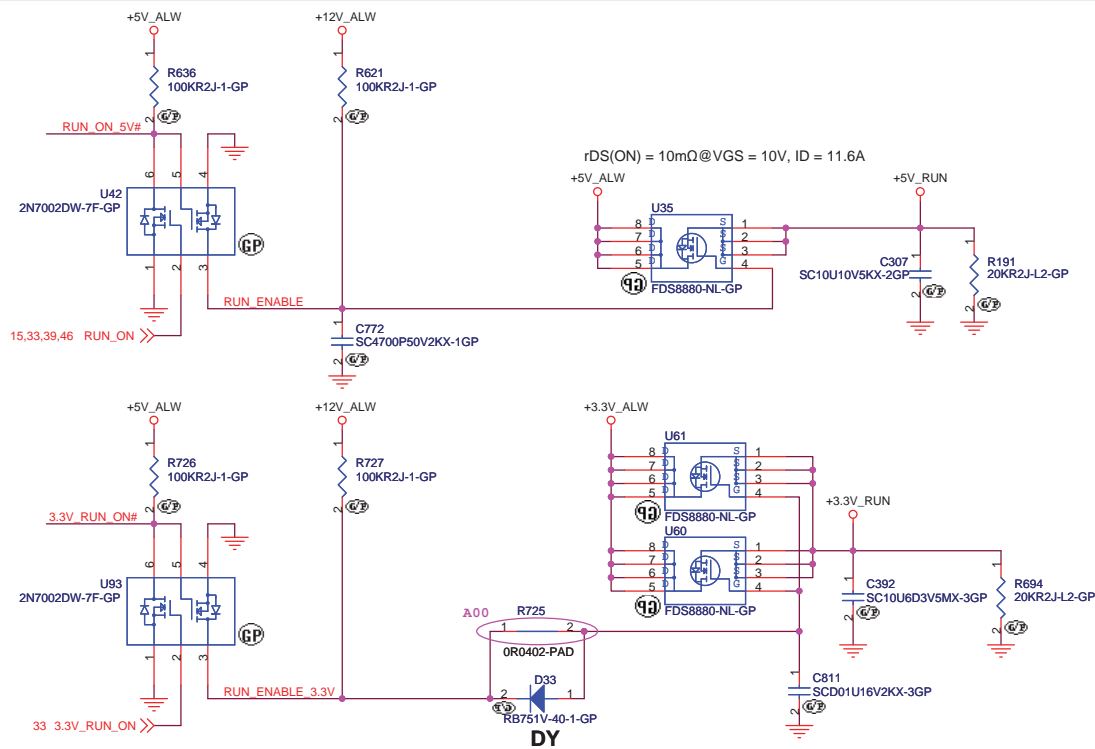


LEFT PANEL LED



RIGHT PANEL LED





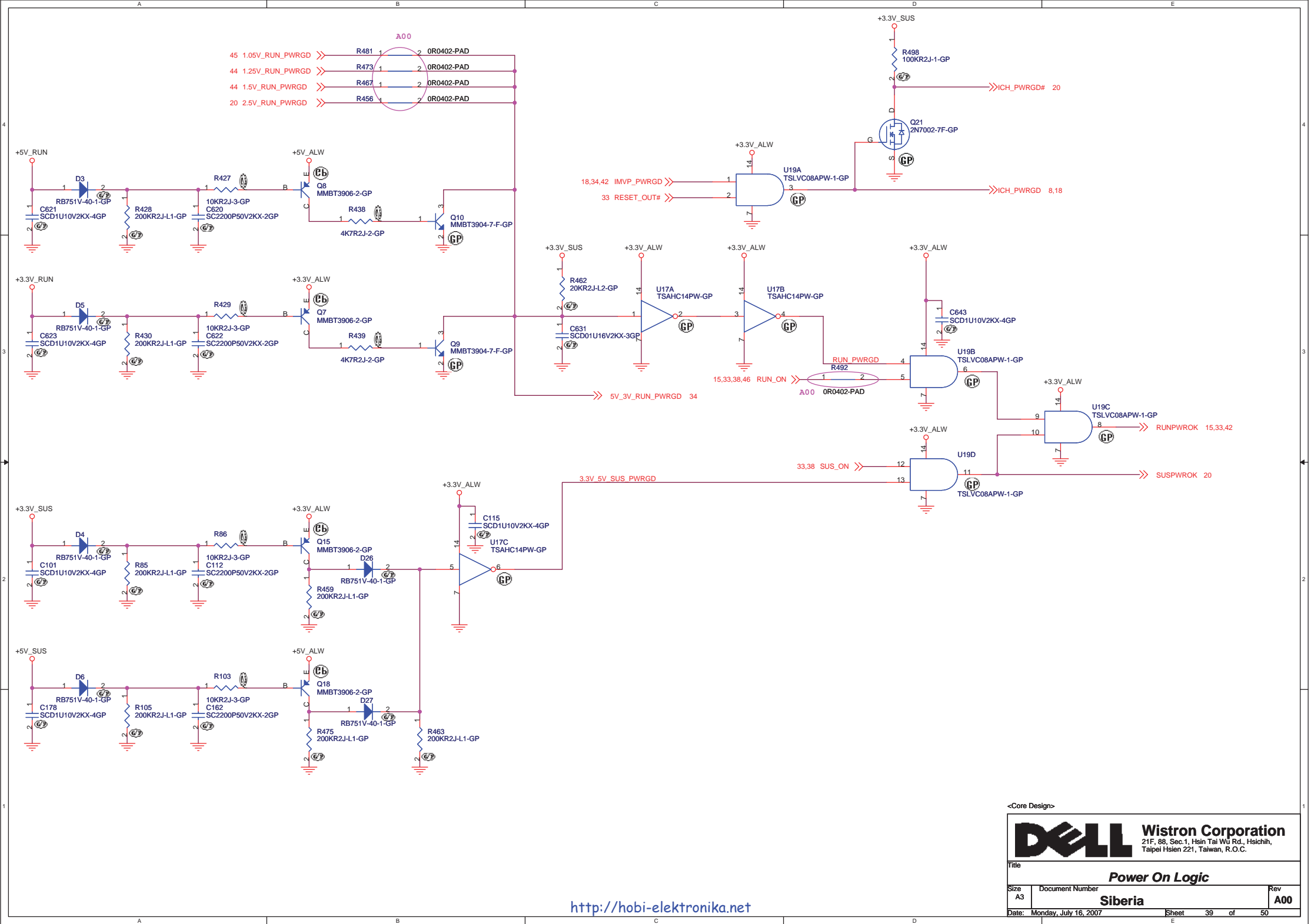
Reserve discharge path

CRB 0.95:
 Insures that +1.05_VCCP and +1.5_RUN ramp
 down together by discharging +1.5V_RUN into
 +1.05V_VCCP

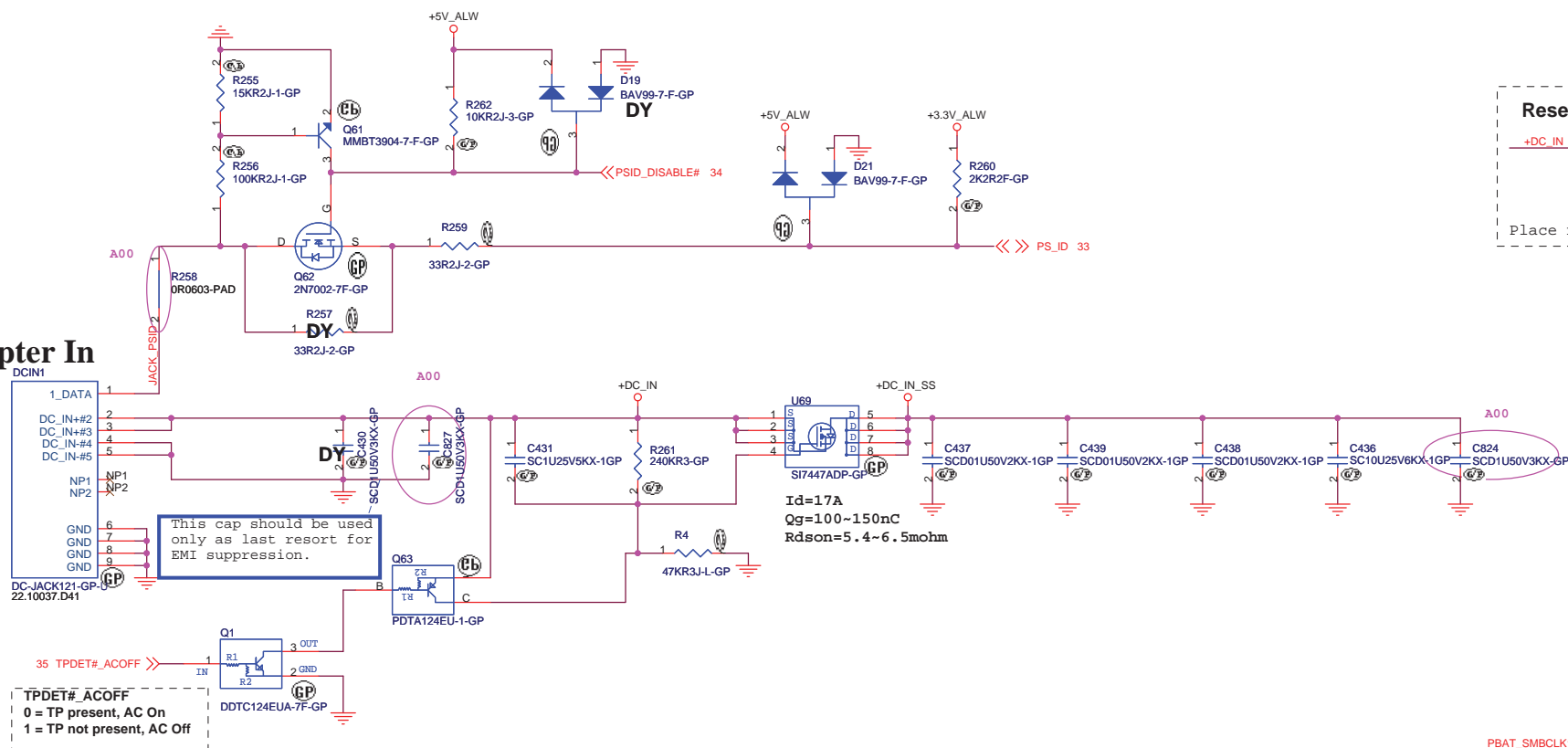
<Core Design>

DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title		
Power Plane Enable		
Size	Document Number	Rev
A3	Siberia	A00
Date:	Monday, July 16, 2007	Sheet 38 of 50



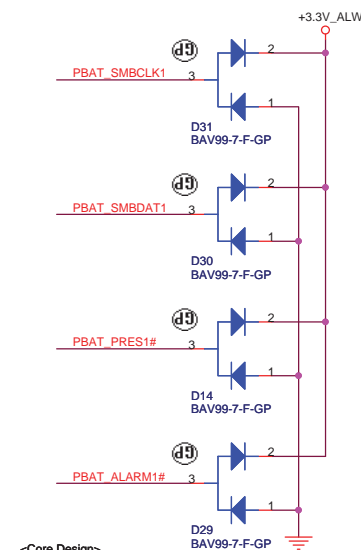
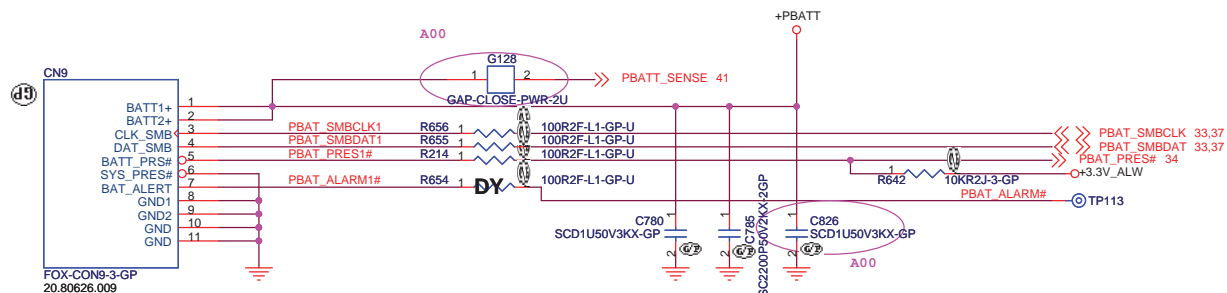
Adapter In



Reserved for EMI



Batt Connector



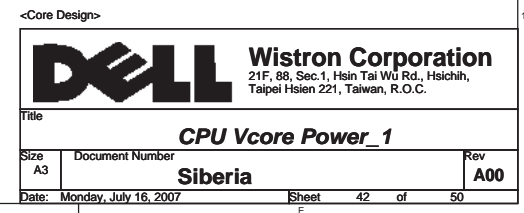
<Core Design>

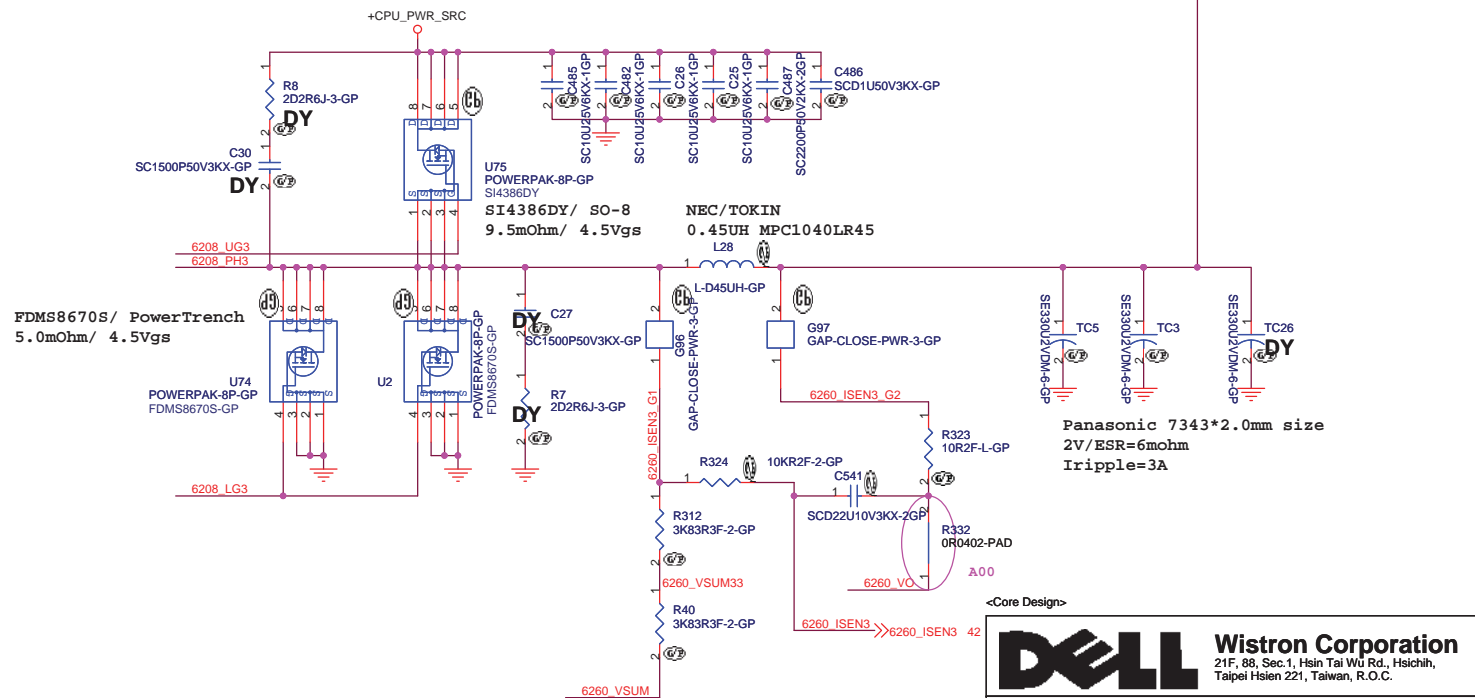
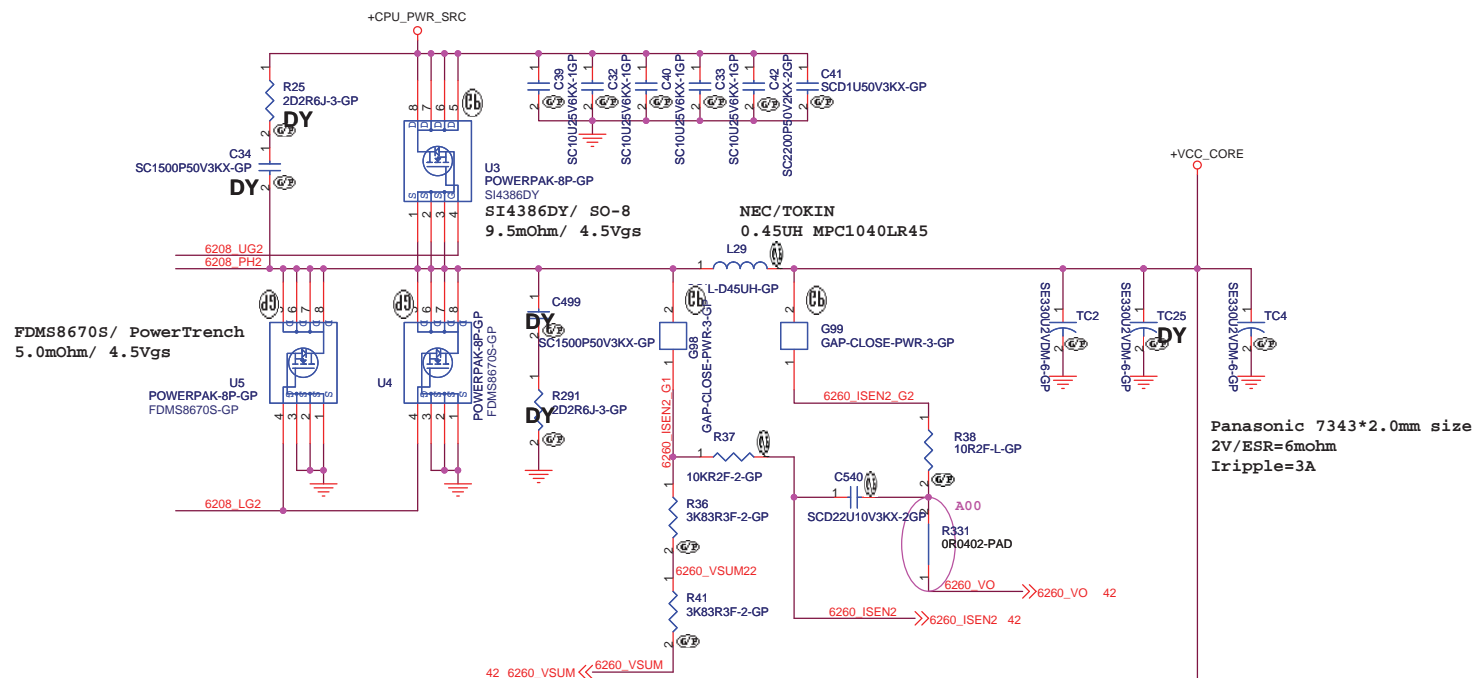
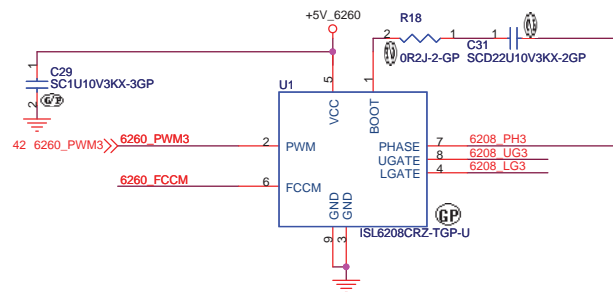
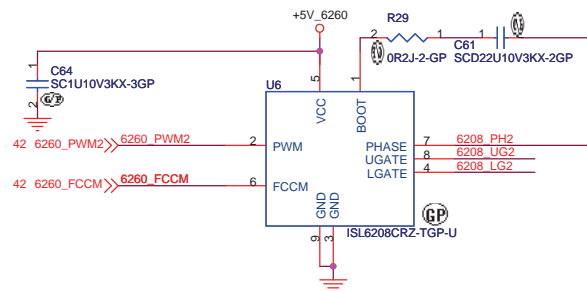
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
DCIN / BATT CONN.

Size A3 Document Number Siberia Rev A00

Date: Monday, July 16, 2007 Sheet 40 of 50

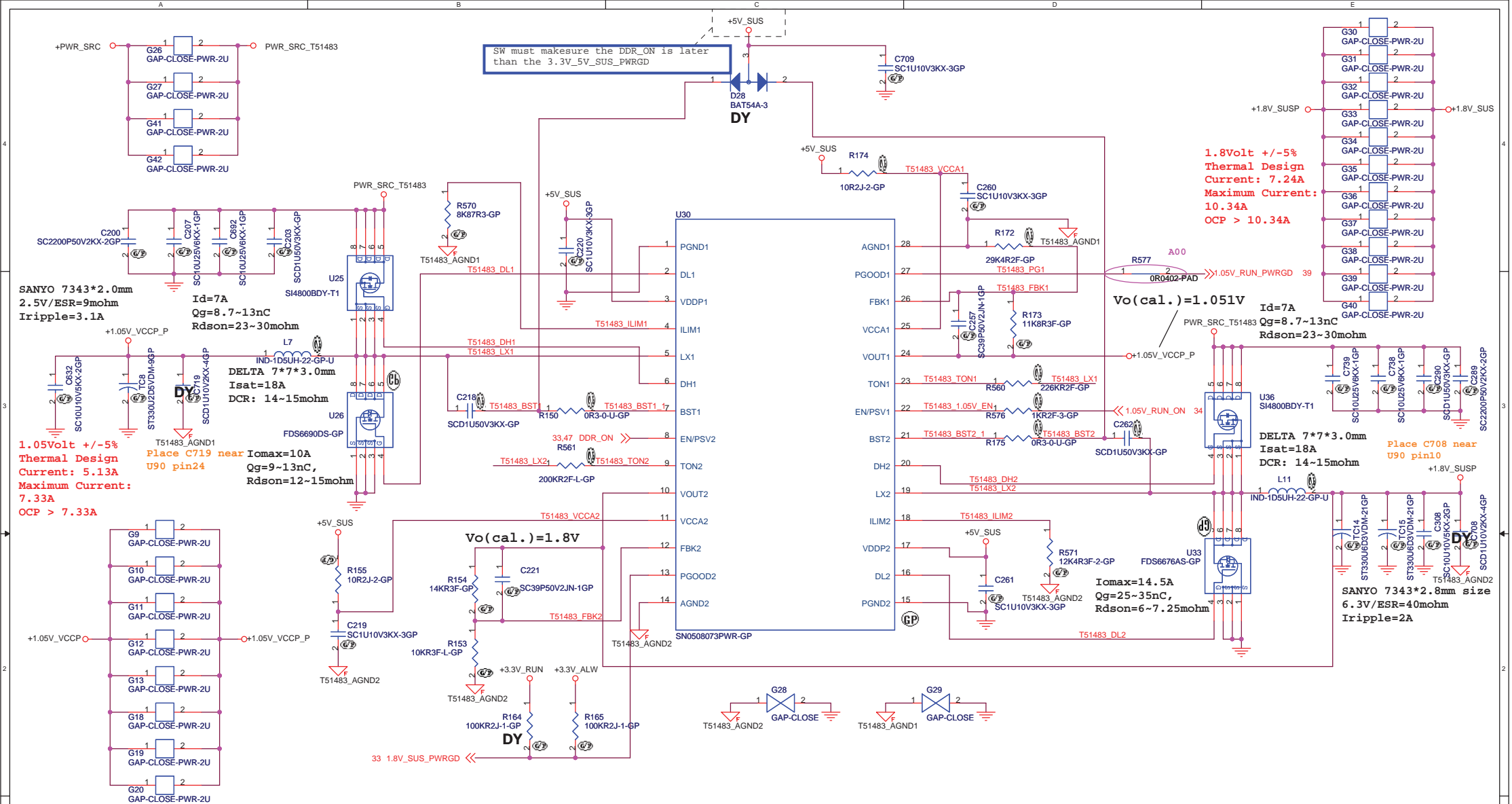




<Core Design>



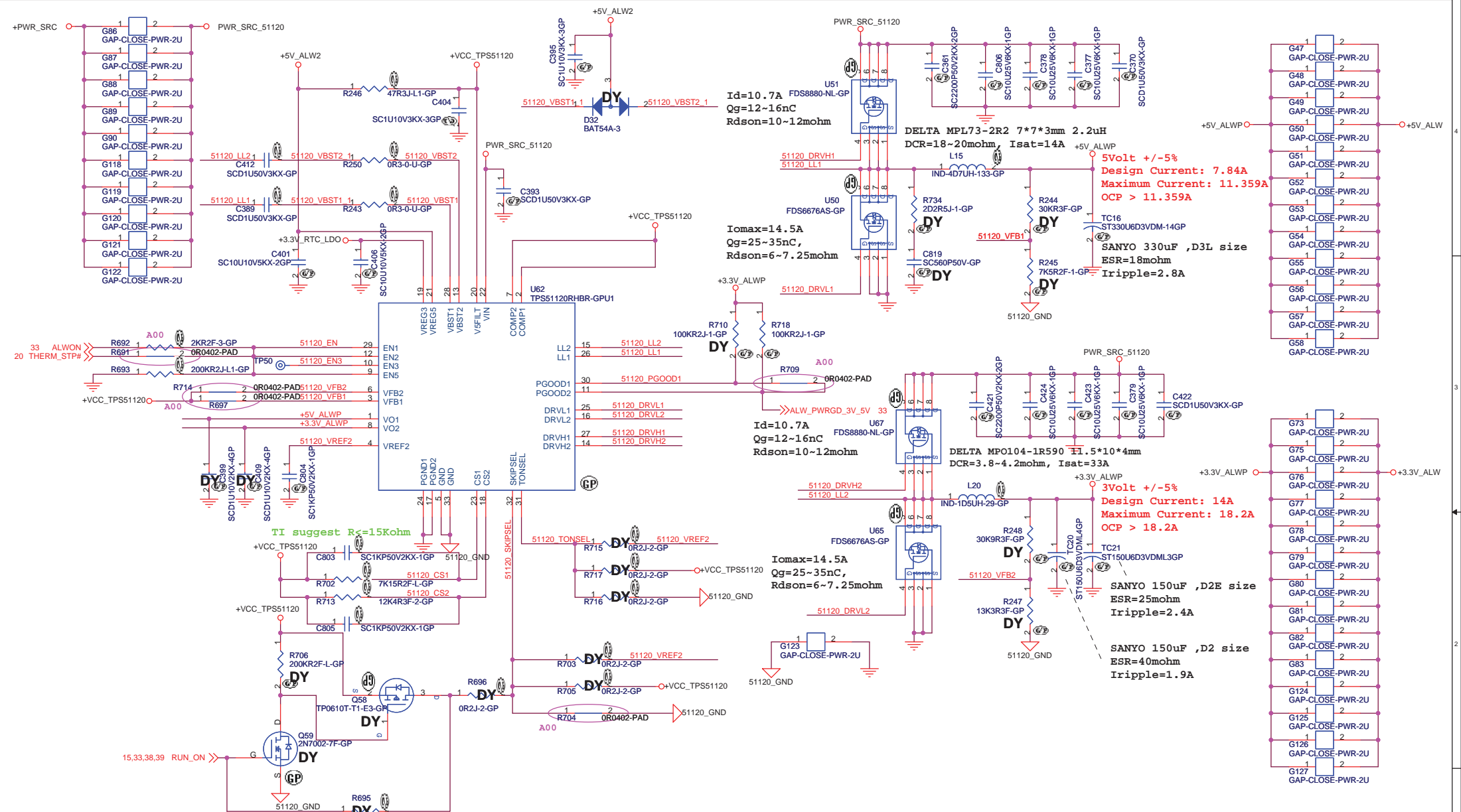
Title			CPU Vcore Power_2	
Size	Document Number	Rev		
A3		Siberia		A00
Date:	Monday, July 16, 2007	Sheet	43	of 50



$$V_{trip}(mV) = R_{trip}(Kohm) * 10 (\mu A)$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/2 * L * f) * ((V_{in} - V_{out}) * V_{ou}) / V_{in})$$

$$V_{out} = (1 + (R_{top}/R_{bottom})) * 0.75$$



	GND	VREF2	PILOT	VSPILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Switcher ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on

$V_{out}=1V \cdot (R1+R2) / R2$

<http://hobi-elektronika.net>

Wistron Corporation

21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

DC to DC 3.3V / 5V

Rev A00

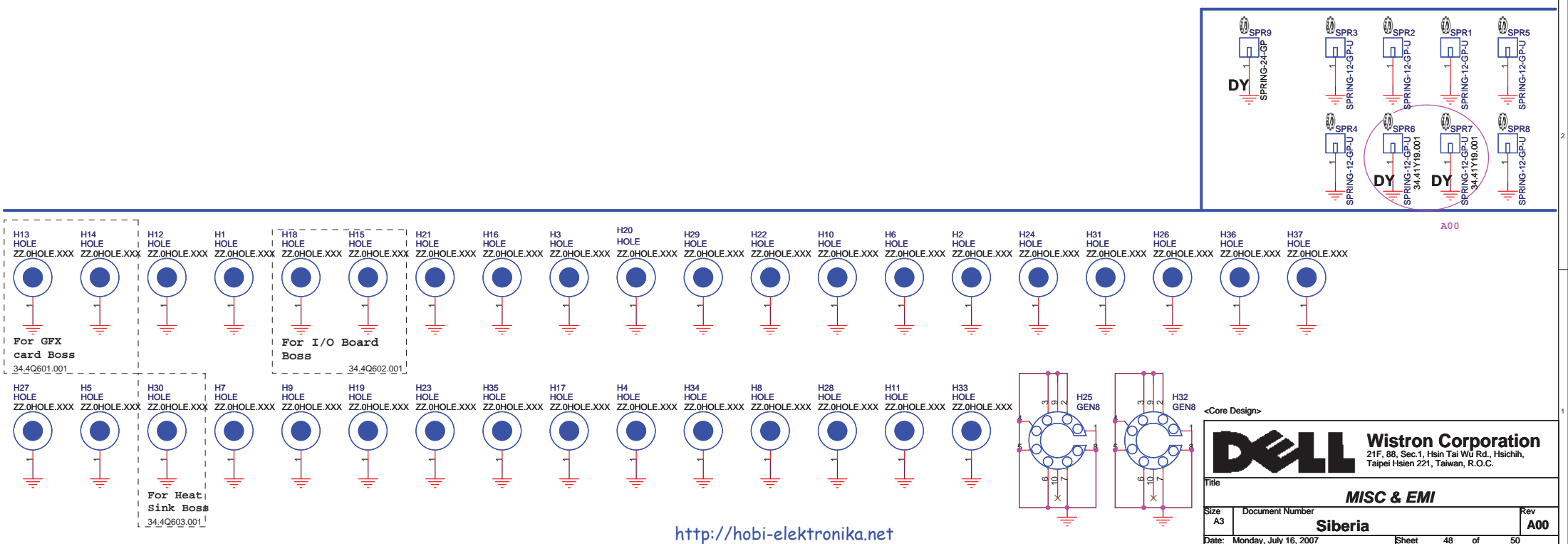
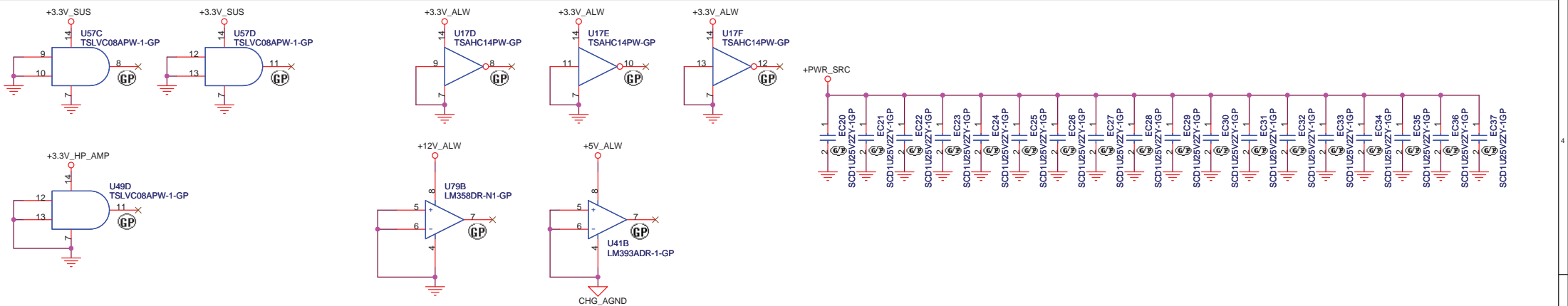
Size A3

Document Number

Date: Monday, July 16, 2007

Sheet 46 of 50

Rev A00



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

MISC & EMI

Siberia

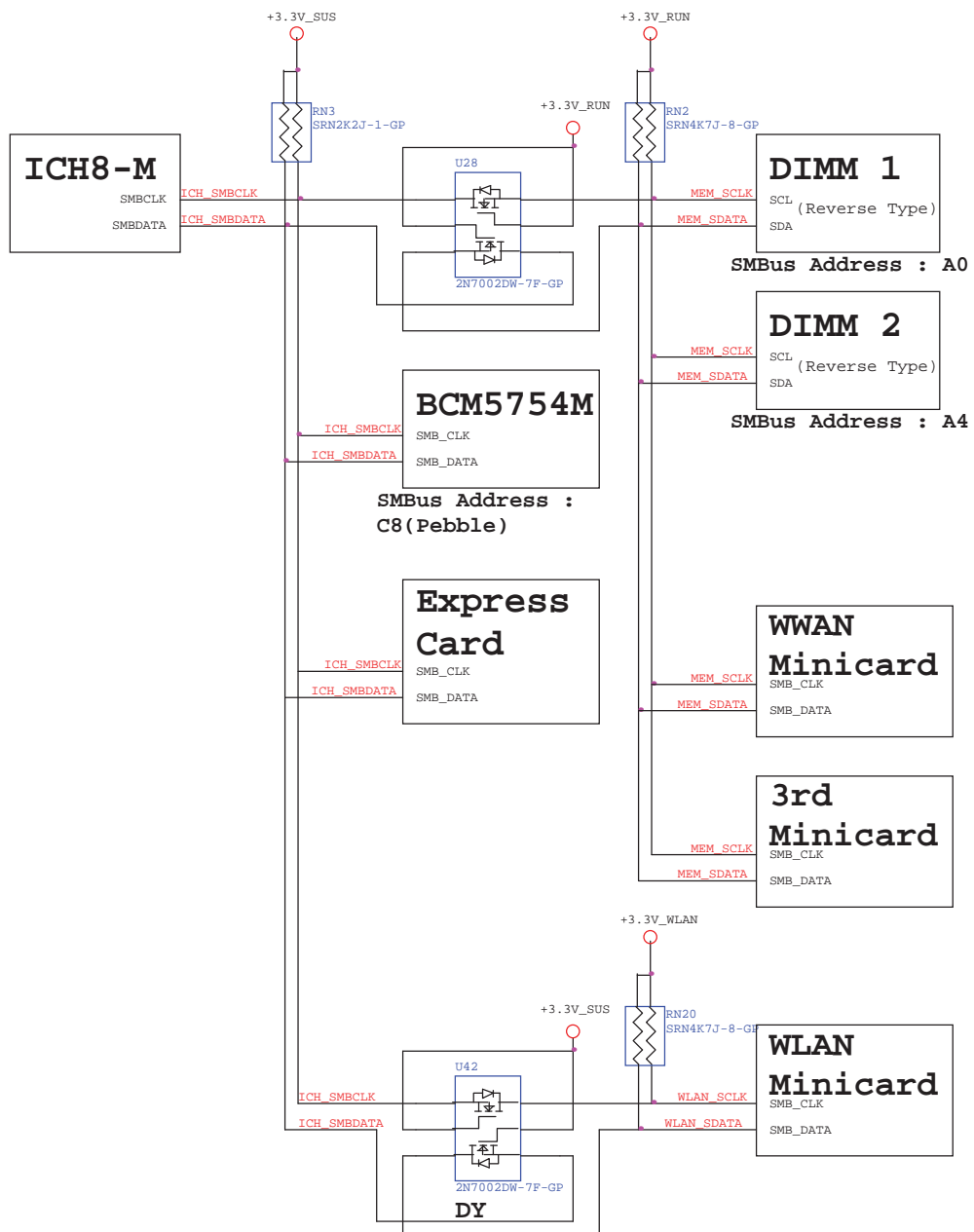
Rev A00

Document Number

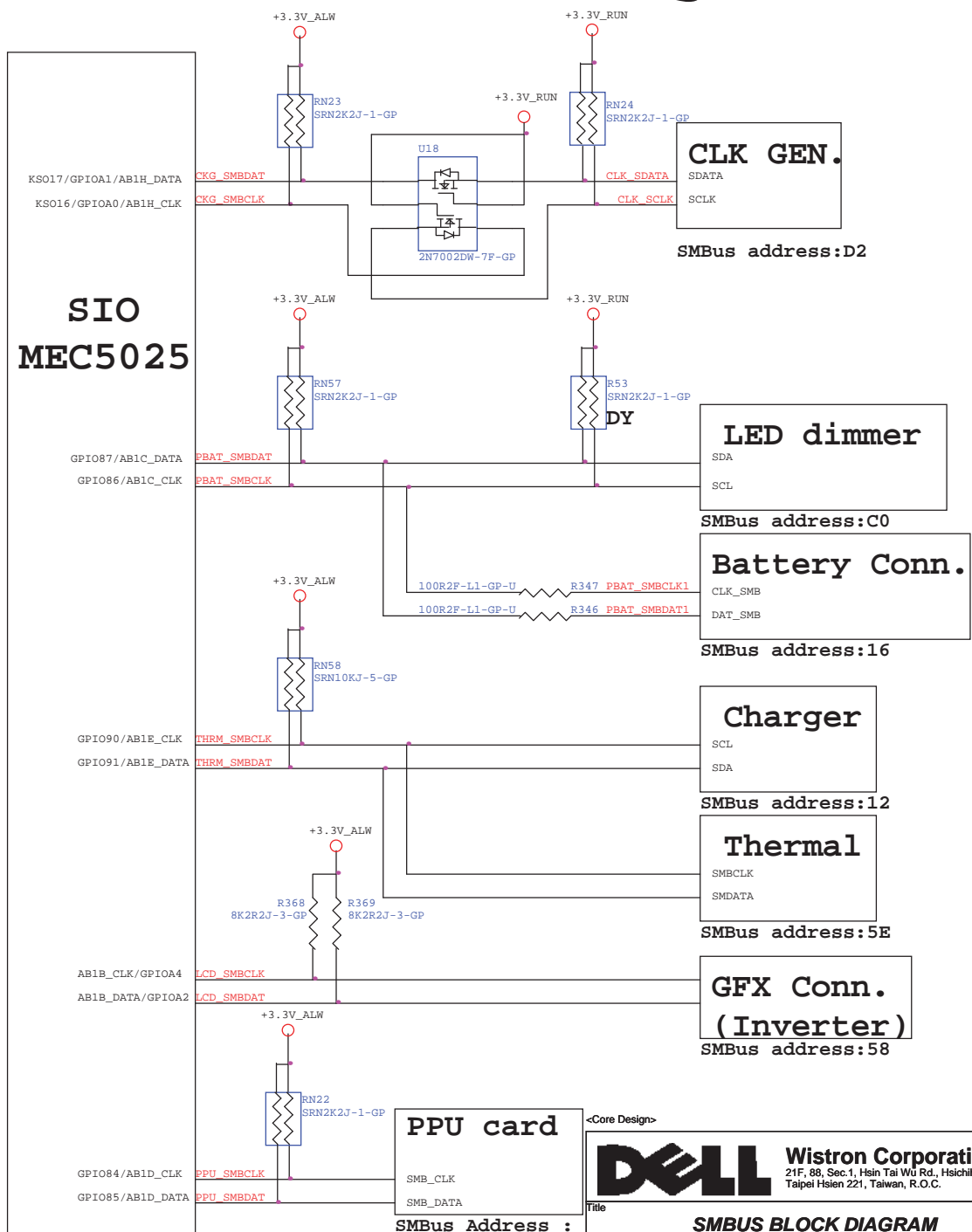
Date: Monday, July 16, 2007

Sheet 48 **of** 50

ICH8 SMBus Block Diagram




KBC SMBus Block Diagram



DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2007/07/12	X02 to A00	1	19	Change C245 from 0.1U 0402 size to 1U 0603 size. (BITs ID: SCH159348)	Dell's command for ICH8 VREF power sequence glitch.	EE
		2	34	Populate R407 and non-populate R388.	Change board ID from X02 to A00.	EE
		3	36	Change U16 to vendor MXIC.	Because SST have shortage issue.	EE
		4	48	Non-populate SPR6, SPR7.(BITs ID: SCH159349)	Can't touch case.	EE
		5	4	Populate C661, C694 to 10p 50V 0402 size. Populate C693 to 8.2p 50V 0402 size.	Solution for 33MHz EMI issue.	EE
		6	4	Purge ICS CLK gen. and put Cypress at main source.	ICS CLK gen. has warn boot issue.	EE
		7	24	Add R739 10K ohm pull-high to +3.3V_RUN.(SCH159171)	For audio AUD_EAPD#.	EE
		8	41	Remove C354 and C358, add C821 as 4.7U 25V 0805.		EMI
		9	15	Add C823 as 0.1U 50V 0603 for +GFX_PWR_SRC.		EMI
		10	40	Add C827 as 0.1U 50V 0603 for +DC_IN.		EMI
		11	40	Add C824 as 0.1U 50V 0603 for +DC_IN_SS.		EMI
		12	40	Add C826 as 0.1uF for +PBATT. Change R218 to close gap.		EMI
		13	28	Populate C434 and C435 as 47pF, non-populate R265. Change L21 to 2500ohm bead.		EMI
		14	27	Change R285 from 1.24K ohm 5% to 1.27K ohm 1%. Change C449 and C461 to 47pF, C447 to 4.7uF.		EMI
		15	31	Non-pop R588, R590.	Command from DELL wireless team.	EE
		16		Change many 0ohm resistors to wire pad.		EE

<Core Design>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		Title	
		HISTORY from X00 to X01	
Size A3	Document Number		Rev A00
Date: Monday, July 16, 2007	Sheet 50 of 50		Siberia